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Research Paper

To study high performance analysis of surround gate SOI MOSFET

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Abstract

In this paper, we are presenting a rigorous study about SOI MOSFET devices development. The development of SOI devices based on gate structure from single gate to surround gate is presented in this paper. We compared the various electrical characteristics between Single gate, double gate, and bulk and also discussed the device modeling based on surround gate structure.

Keywords: *Soi Mosfet, Surround Gate, Fd Soi Mosfet.*

1. Introduction

Since the advent of MOSFET technology, reducing or scaling down its dimensions has been of main focus. In the past few years, it was observed that reducing the device dimensions improves the performance of device and the circuit speed increases due to scaling of density and further, less power is consumed by the circuit and it occupies less area [1-2]. Scaling increases speed and density of a device but it degrades the performance of the device [3]. So, to deliver better performance, keeping leakage in control, complex steps have been added in the silicon transistor manufacturing, which becomes very costly and time consuming [4].
To overcome this, SOI technology was developed in 1964. SOI increases functionality of chip without the cost of process changes.

2. Device Structure of Soi Mosfet

The basic structure of an SOI MOSFET is depicted in figure.

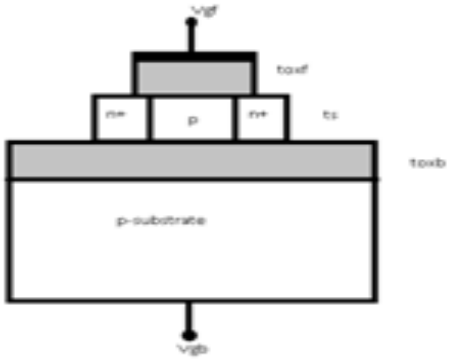

Fig.1: Basic Structure of SOI MOSFET

We fabricate the device on a thin film of single crystal silicon, and it is separated from the silicon substrate by an oxide layer. The source and drain junctions extend all the way to this oxide so, the junction capacitance is very low. A buried oxide insulation layer also reduces current leakage from the drain/source junction to substrate [5]. Also, there is an oxide isolation between the active region and the substrate, parasitic capacitance is also low [6].The insulation layer introduces lower coupling capacitance from the conducting channel to the substrate compared to bulk MOS [7-8]. It is seen that using SOI MOSFET reduces power dissipation up to 66% compared to the conventional bulk MOSFET. And, for the same power dissipation, up to 35% improvement in operating frequency can be achieved [9].

Unlike CMOS, SOI are not doped with any kind of impurities and reduce a lot capacitance. So these operate at faster rate (higher mobility) [10]. Also, SOI MOSFETs are used widely in space applications because they are less sensitive to radiation damage.

An SOI MOSFET can be considered as a combination of two MOS structures – the front gate, (front gate oxide(FOX) and silicon film constitute the front MOS) [11] and the back gate (buried oxide (BOX) and silicon film constitute the back MOS).

SOI MOSFET can be classified into two categories namely:

1. Partially depleted (PD) and
2. Fully depleted (FD).

In a **Partially depleted SOI MOSFET**, the sandwiched p type between FOX and BOX is quite large and thus, the depletion region can not cover the whole p region. In PDSOI, problem of floating body effect is seen.

In **Fully depleted SOI MOSFET,** p sandwiched region is very thin and hence, the depletion region covers the whole film.

Fully depleted SOI is mostly used, buried oxide reduces parasitic capacitance between source and drain and confines electron flowing from source to drain reducing leakage current [12].

FDSOI has many advantages like low parasitic capacitance, better threshold swing, etc

3. Device Structure (Based On Gates)

Single Gate : As the name suggests, these devices have only one gate, which means that there is a single gate which is controlling the flow of electrons in the channel. This is similar to the conventional MOSFET where single gate is present.

Double Gate : These devices have two gates for simultaneously controlling the charge in the silicon body layer, allowing two channels for current flow. The two gates are present at the front and the back end. There is charge coupling between the front and back gate [13].

Multigate : These devices, as the name suggests have more than two gates. These can have three gates – tri gate or four and so on. Here more gates are present to control the flow of charge in the channels.

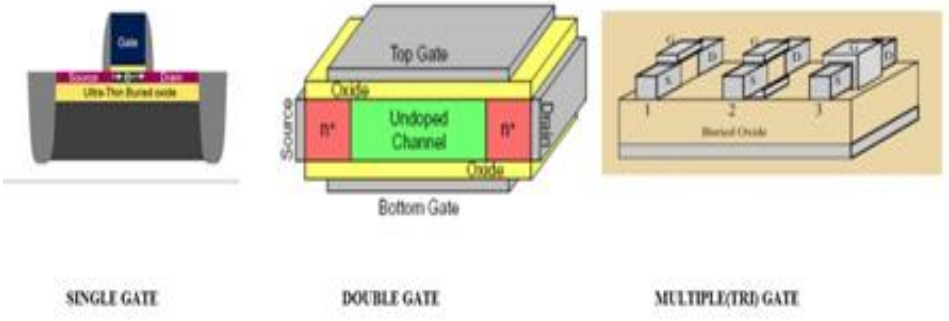

Fig.2: Single, Double, Triple gate SOI MOSFETs

Comparison of various characteristics of SOI, BULK, DG can be shown as [14]

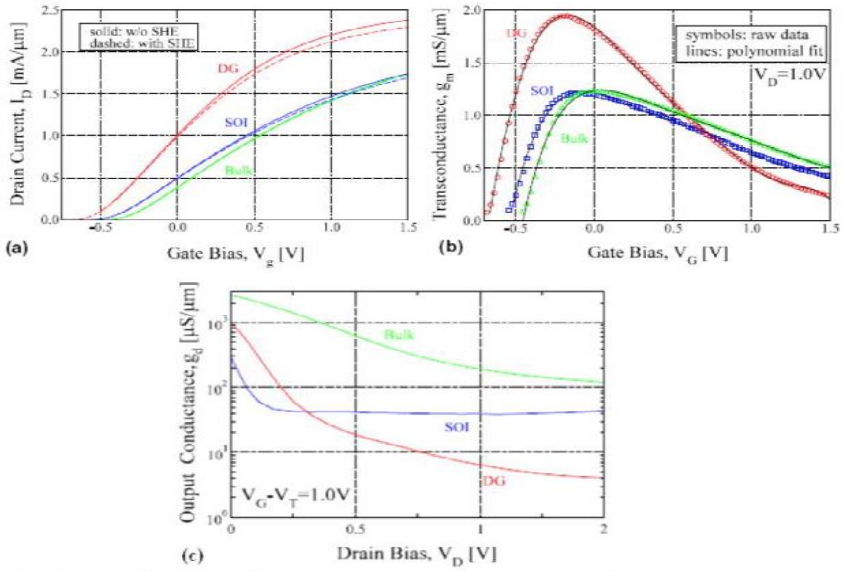

Fig. 3:(a) I_g-V_g Characteristics (b) Corresponding transconductance curve for the same devices (c)Drain –bias dependence of g_d is typically low in saturation but non zero

Surround Gate : The main problem in the above discussed devices is their control over the charge flow in the channel. So, for better control over the channel we can use surround gate SOI MOSFET. In surround gate devices, channel is covered by gate from all sides. It is somehow similar to a FinFet. Besides providing better control over the charge flow in the channel, it also provides better accuracy.
Basic structure of surround gate can be shown as:

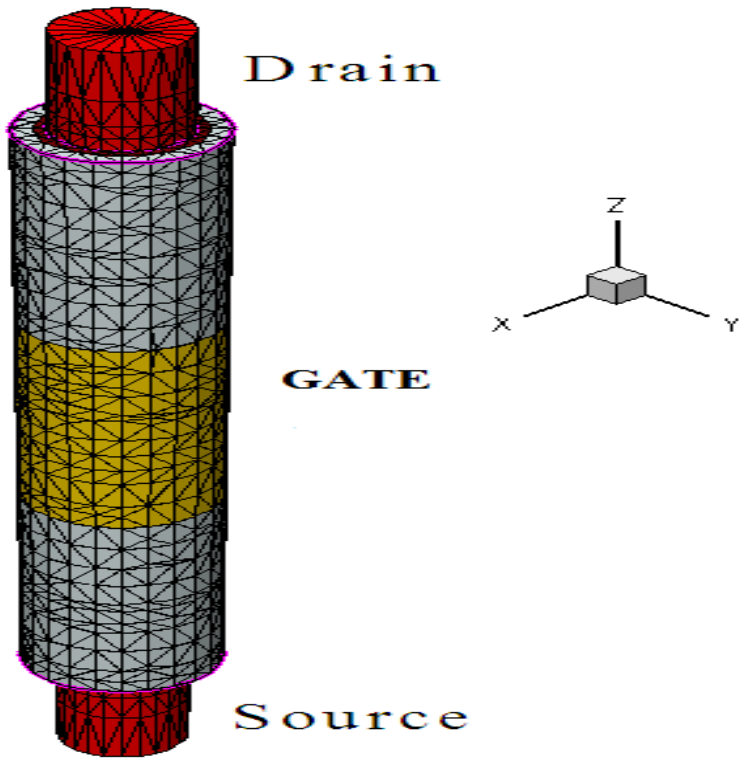

Fig.4: Surround gate Soi Mosfet

4. Device Modeling of Soi Mosfet

Many methods were used to calculate the surface potential like Green's function method, Poisson's 3D equation, Uniform parabolic function, etc.
We will use Poisson's 2D equation to evaluate Surface potential and threshold voltage. The 2D Poisson's equation is a useful approach to calculate potential by relating potential to the charge density which gives rise to it.
The divergence relationship relates Electric field to the charge density as:

$$\nabla . E = \frac{\rho}{\varepsilon_0}$$

And we know, Electric field is related to potential by the equation:

$$E = \nabla . V$$

Therefore, potential can be related to charge density as:

$$\nabla . \nabla . V = -\frac{\rho}{\varepsilon_0}$$

The 2D poisons equation in the cylindrical coordinates is given by [15]

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial(\emptyset(r,z))}{\partial r}\right) + \frac{\partial^2(\emptyset(r,z))}{\partial z^2} = \frac{qN_A}{\varepsilon_{si}} \quad (1)$$

Where$\emptyset(r,z)$ is the potential in the channel and$\varepsilon_{si}$is the permittivity of silicon,q is the unit charge in coulombs.

The device structure and characteristics will be constructed, examined and simulated using Silvaco Atlas. We will also be using Mathcad.

5. Conclusion

To increase the performance of the device, the control of the electrons inside the channel is more essential. The single gate and double gate provides the control inside the channel via 1 gate or 2 gate and provides enhanced control. To increase more precise control over the channel, the development of surround gate devices is done. In surround gate devices, channel is covered by gate from all sides. Besides providing better control over the charge flow in the channel, it provides better accuracy.

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