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Research Paper

Design of voltage level shifter for power-efficient applications using 45nm technology

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Abstract

The paper describes a voltage level shifter for power efficient applications which is simulated in tanner spice tool using 45nm technology. The conservative voltage level shifter is designed by using 6 transistors. The voltage level shifter cell generally used for shifting the voltage range of the signal from one voltage domain to another. This is required when the chip operate at multiple voltage domains. The circuit parameters like leakage voltage and average power dissipation are calculate for this circuit. Mainly level shifter consists of two voltage levels. One is low logic supply voltage (VDDL) another one is high logic supply voltage (VDDH). The simulation results of proposed level shifter with Wilson current mirror by 45nm technology for the input frequency of 1MHZ, the power dissipation of 0.177nW with 3db gain of 9.78.

Keywords: *Conventional Level Shifter; Dynamic Level Shifter; Leakage Voltage; Level Shifter with Wilson Current Mirror; 45nm Technology; Voltage; Power Consumption; Gain and Gain Bandwidth Product (GBW).*

1. Introduction

Developments in manufacturing processes of semiconductor fabrication have permitted only for smaller geometries in the designing of circuit along with lower levels of supply voltage. This development in the technology supports many of the low-power and high-performance applications presently being designed. The existing technology could not be able to support these new designs. Hence to make use of these new designs by means of existing technology, there should be a means towards matching of output voltage level of one device with the input voltage level of another device in the circuit design as given in Figure 1. Various options are available to achieve this requirement of design.

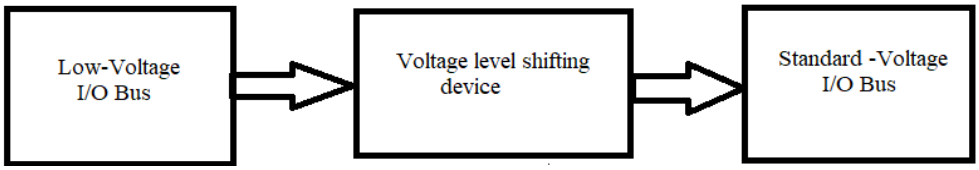


Fig. 1: Block Diagram of Voltage Level Shifter.

The different types of technologies presented in the design of circuit decide the threshold of input voltage along with achievable output voltage levels in various devices. To establish connection between two devices offered by different technologies effectively, translation of voltage level might be required. These requirements consist of

1) The driver device high-level output voltage should be greater than the receiver device high-level input voltage.
2) The driver device low-level output voltage should be less than the receiver device low-level input voltage.
3) The output voltage level of the driver device should not go beyond the Input/output voltage tolerance of the receiver device.

In digital Electronics, level shifter is also called as a logic-level shifter. This circuit is used to convert signals from one logic level or voltage domain to another logic level or domain, which allows compatibility between different ICs with different voltage requirements, like TTL as well as CMOS. Many of the contemporary full-featured systems make use of the level shifters to bridge the domains amongst the low-power application processors working with 1.8 V and other system functions such as sensors or analog concentrated applications working with 3.3 or 5V.

2. Types of level shifters

1. Uni-directional level shifters – in this type of level shifters all the pins available at the input are devoted to one voltage domain while all the pins at the output are devoted to the other. 2. Bi-directional level shifters with Dedicated Ports – every voltage domain have both the input in addition to the output pins, but the direction of data pin does not change. 3. Bi-directional level shifters with External direction indicator – The alteration in external signal decides the output in this type of level shifters. When there

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is a change in an external signal, inputs turn out to be outputs and vice versa. 4. Bi-directional level shifters, auto-sensing – A pair of I/O spanning voltage domains be able to operate as either inputs or outputs depending on the external stimulus exclusive of the need meant for a committed direction control pin. Generally, in an Integrated Circuit, both analog and digital voltages are present. If the signal transmitted from digital to analog then it comes under voltage up-level shifter and If the signal transmitted from analog to digital then it comes under voltage down-level shifter. After a general introduction of level shifter, Conventional level shifter has been discussed in section II. And Dynamic voltage level shifter has been discussed in section III. And level shifter with Wilson current mirror has been discussed in section IV.

3. Conventional voltage level shifter

In Figure. 2, a Simple Conventional Voltage Level Shifter meant for the chips by means of a low VDDL Voltage at the core and higher VDDH Input/Output voltage. The output driver circuit accepts a low input voltage swing and generates a higher output voltage swing. The output driver circuit makes use of a Cascade Voltage Swing Logic (CVSL) Structure that consists of four high voltage transistors representing in bold. The inverter uses low voltage transistors along with low voltage power supply. The output (out) can be followed by a high voltage inverter to deliver more uniform rise/fall times. The inverter is a receiver which accepts high input voltage swing and produces a lower voltage swing for core circuits. It contains a simple inverter constituted with high voltage transistors which are capable to survive the large gate voltages.

Operation of Conventional voltage level shifter

Conventional voltage level shifter contains two PMOS transistors in pull up device which acts as cross-coupled load. When logic "HIGH" that is VDDL is given to the input signal (IN) , then the pull down NMOS transistors MN1 is ON, so that it provides conducting trail towards the ground and MN2 is OFF, which causes Q2 is pulled down to ground. Whenever Q2 goes to zero then MP1 is in ON condition, so that Q1 is pulled to high that is VDDH. And finally, the resultant output (OUT) goes low. As input signal (IN) becomes "LOW" condition the reverse operation comes into picture.

The major disadvantage of conventional voltage level shifter is, it would not be able to convert the voltage levels since (IN1 & IN2) << (IP1 & IP2). So, to prevail over this difficulty, the level shifter is designed with static current mirror. But the static current mirror is mainly suffering with static current flow which leads towards the static power dissipation. So, to reduce problem of power dissipation, level shifter circuit is designed using dynamic current mirror. Level shifter or translator is usually connected in a typical Op-Amp so as to shift the D.C. Level at the output of intermediate stage which is grounded onward to zero. Intermediate stage is basically a differential amplifier which is driven by the previous state output. The D.C. Level at the output of intermediate stage is good above ground potential in case of direct coupling. Hence, it is obligatory to use the level shifter in OP-Amps.

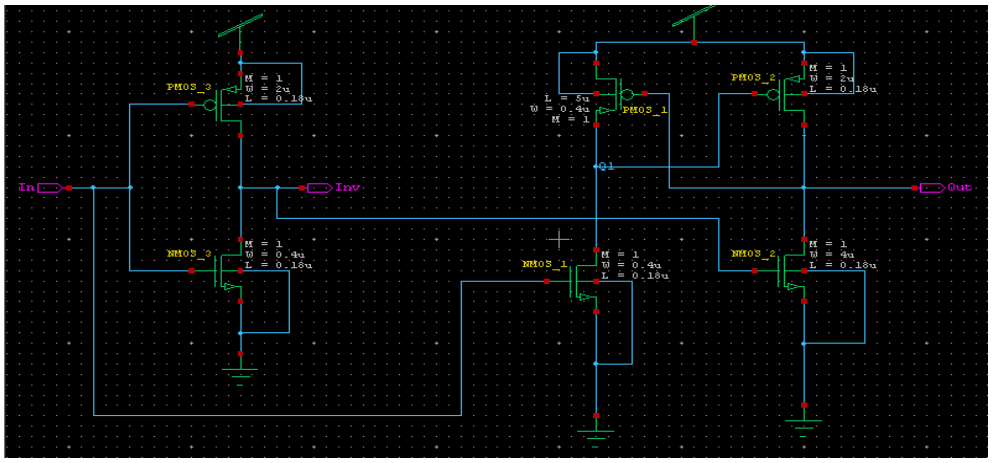


Fig. 2: Schematic of Conventional Voltage Level Shifter.

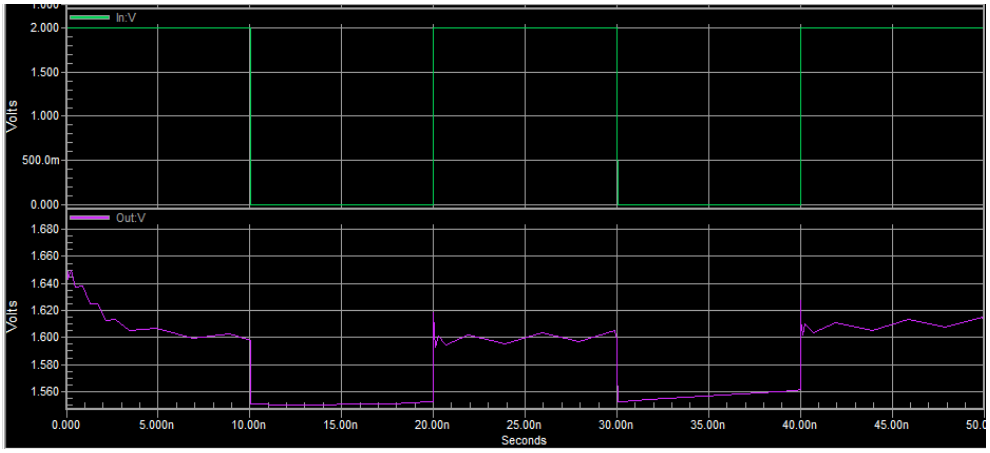


Fig. 3: Voltage vs. Time Waveforms of Conventional Level Shifter.

Advantages of conventional level shifter is, it is having high performance, low power consumption and also static and dynamic power will reduce by the use of low voltage levels. The main disadvantage is, it is having high propagation delay.

4. Dynamic voltage level shifter

A dynamic level shifter may include a pull-down circuit and a pull-up circuit. The pull-up circuit may include an extra transistor

configured to reduce the current through that circuit when the pull-down circuit is activated. A ring oscillator may be implemented using instances of the dynamic level shifter along with instances of a static level shifter. In one embodiment, a dynamic level shifter circuit may receive an input signal referenced to a first voltage of a first power domain, and may output a corresponding signal referenced to a second voltage into a second power domain. The dynamic level shifter circuit may include an evaluation node that is precharged during a first phase (e.g., the low portion) of a clock signal. During the second phase (e.g., the high portion) of the clock signal, the evaluation node may be either pulled low or high, depending on the state of the input signal. A corresponding output signal, based on the evaluated level on the evaluation node, may be output into the second power domain.

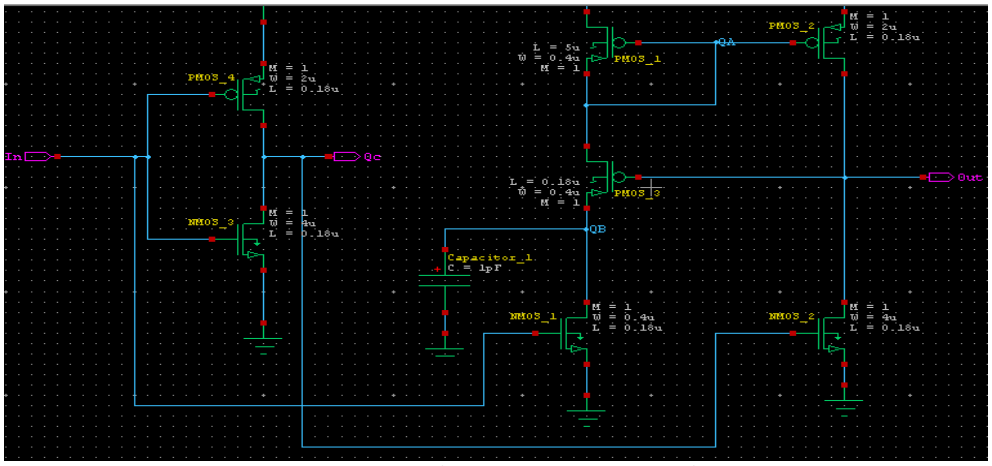


Fig. 4: Schematic of Dynamic Voltage Level Shifter.

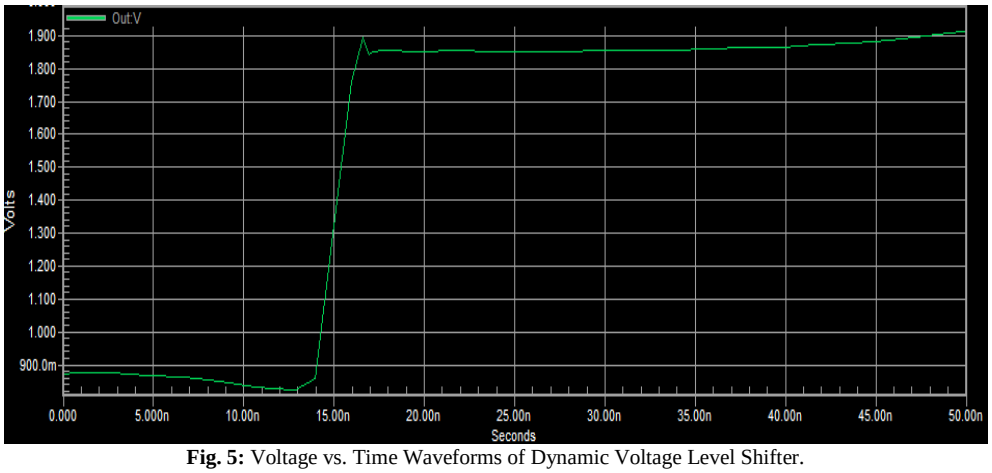


Fig. 5: Voltage vs. Time Waveforms of Dynamic Voltage Level Shifter.

5. Voltage level shifter with Wilson current mirror

This is the current mirror with feedback. It will give stable output currents for wide voltage swings and enhanced output impedance. Mainly the Wilson current mirror consists of four transistors M1, M2, M3 and M4 and M1 is separately biased with Vbias so that Vbias is biasing voltage which bias the M1 transistor and it is having fixed voltage. Whenever Vbias is fixed, the current which flows through M1 transistor is also fixed. So, the same amount of current is flowing through the transistor M2, M3 is diode connected transistor and M4 is simple output transistor.

Operation of Wilson current mirror

As the output voltage (Vo) increases, which causes output current (Io) increases because of channel length modulation. Which makes current (ID2) in M2 transistor will increases, so as to reduce the source and drain voltage (VDS2) of M2 transistor that is voltage at point A will reduces. Which makes gate and source voltage (VGS4) of M4 transistor will reduces. So finally, the output current (Io) will reduce. In this way the output current (Io) is stabilized.

The major advantages of Wilson current mirror is, because of negative feedback the drain current is stabilized. And current series sampling is used at the output to increase the output impedance.

Nonetheless Wilson current mirror circuit comes with limitations like

The least potentials from input or output to the general rail connection that are required in favor of good operation are more superior than for the standard two-transistor mirror. This reduces the headroom accessible to produce the input current along with limiting the compliance of the output. Hence making the operable conditions in favor of requirements.

This mirror makes use of feedback to increase the output impedance in such a way that the output transistor contributes collector current variation noise to the output. All three transistors of the Wilson current mirror put in noise to the output. The added noise limits the performance of the circuit which is not desirable.

When the circuit is biased for high frequency operation with utmost{\displaystyle \, the negative feedback loop with the purpose of maximizing the output impedance may cause peaking in the frequency response of the mirror. For stable, low-noise operation it may be necessary to modify the circuit to eliminate this effect.

In some applications of a current mirror, particularly for biasing and active load applications, it is advantageous to produce multiple current sources from a single input reference current. This is not possible in the Wilson configuration while maintaining an accurate match of the input current to the output currents.

Net list for voltage level shifter designed with Wilson current mirror. Include “c:\users\sahithi\desktop\libfiles\45nm.md”
MM2 N_1 N_2 Gnd 0 NMOS W=67.5n L=45N
MM3 N_2 N_2 Gnd 0 NMOS W=67.5n L=45N
MM4 Out N_1 N_2 0 NMOS W=67.5n L=45N
MM1 N_1 in Vdd Vdd PMOS W=135n L=45N
Vdd Vdd Gnd 1.8V
Vin In Gnd pulse (0 1.8V 0 0.05ns 0.05ns 5ns 10ns)
. tran 1ns 50ns
. power Vdd 5ns
.print tran v (in) v (out)
. end

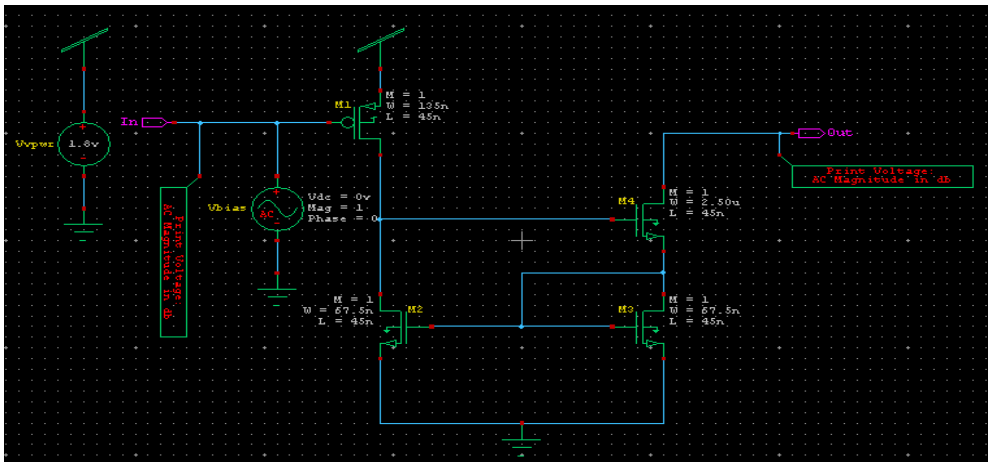


Fig. 6: Schematic of Voltage Level Shifter with Wilson Current Mirror.

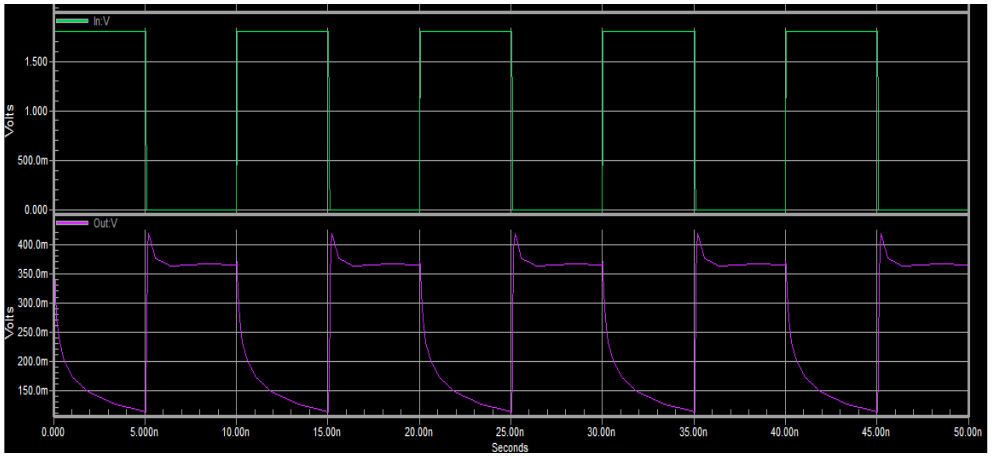


Fig. 7: Waveforms of Voltage Level Shifter with Wilson Current Mirror.

Table 1: List of Various Devices with Their Advantages and Disadvantages

Device	Advantages	Disadvantages
Conventional Voltage Level shifter	* Low dynamic power * Low short-circuit power * High performance * Low power consumption	* High propagation delay * High sensitivity to noise
Dynamic Level shifter	* No static-current leakages	* Delay increases * Power consumption increases
Level shifter with Wilson current mirror	* Low propagation delay * High performance * Current mirror ratio should be large i.e., (W/L) P2/(W/L) P1	

(A)

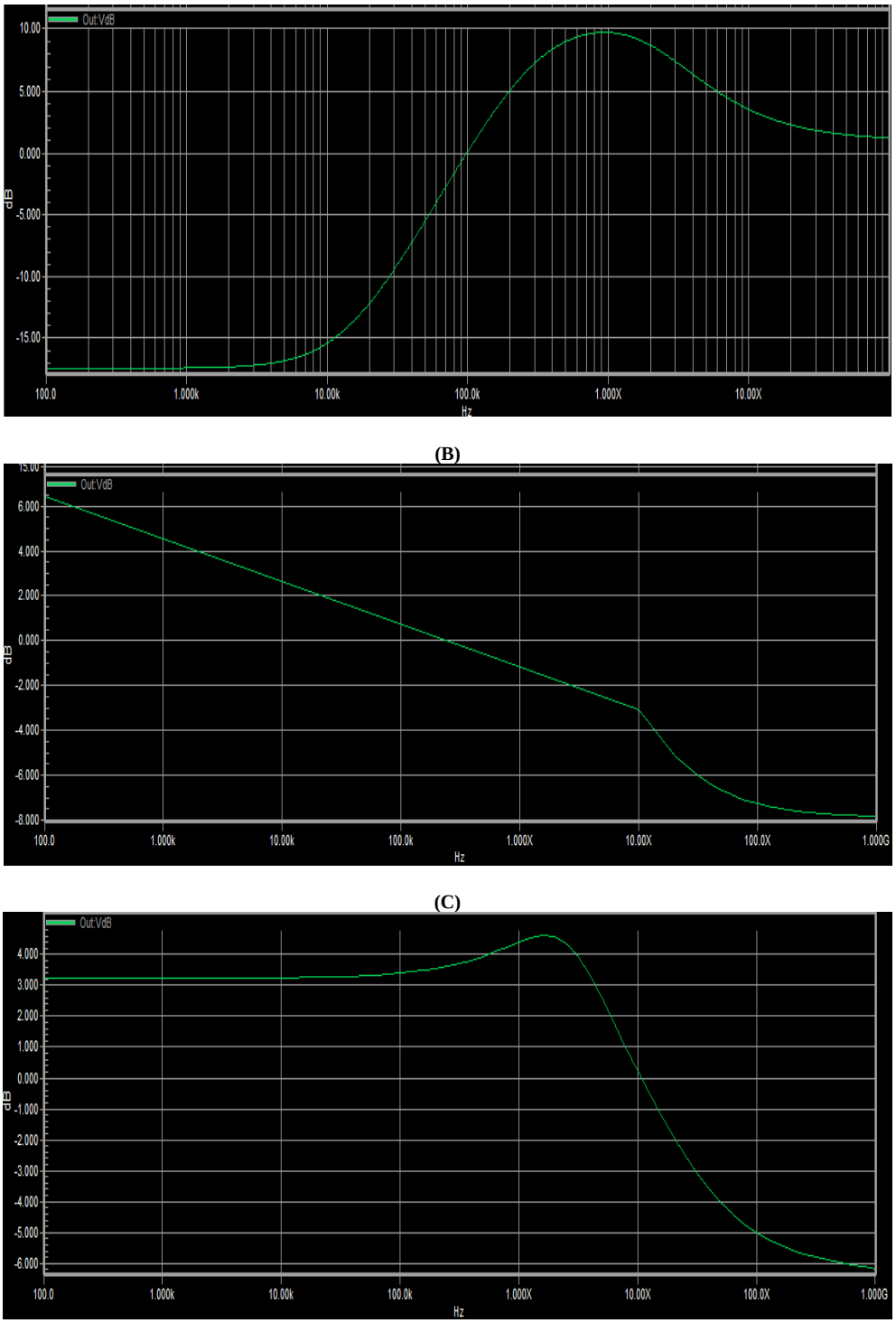


Fig. 8: Simulated Waveforms of Voltage Level Shifter A) Gain vs. Frequency of Voltage Level Shifter Designed with Wilson Current Mirror B) Gain vs. Frequency of Dynamic Level Shifter C) Gain vs. Frequency of Conventional Level Shifter.

Table 2: Comparative Simulation Results for Voltage Level Shifters

	Conventional Level Shifter	Dynamic Level Shifter	Level Shifter with Wilson current mirror
Technology	180nm	90nm	45nm
Supply Voltage	1.8V	0.9V	0.7V
Frequency	1MHZ	1MHZ	1MHZ
Power dissipation	0.17mw	0.49uW	0.177nw
Gain <3dB>	4.61	6.42	9.78
Bandwidth	10.6MHZ	6.07MHZ	988KHZ
Gain bandwidth Product (GBW)	49MHZ	37MHZ	967KHZ

6. Conclusions

In this paper, the architecture of Voltage level shifter is proposed with Wilson current mirror by using 45nm CMOS technology, which is mainly able to shrink the power consumption as well as greatly improves the gain of circuit. The simulation results verified the power dissipation, gain, bandwidth, and gain bandwidth product (GBW) of the proposed voltage level shifter circuit with other level shifters.

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