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Research Paper

A VLSI implementation of elevator control based on finite state machine using Verilog HDL

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Abstract

In this cutting edge period, lifts have turned into a basic piece of any business or open complex. It encourages the quicker development of individuals and gear between floors. The lift control framework is a standout amongst the most critical perspectives in hardware control module that are utilized as a part of car application. Normally lifts are intended for a particular building considering the fundamental factors, for example, the tallness of the building, the quantity of individuals venturing out to each floor and the normal times of high utilization. The lift framework is composed with various control procedures. This usage depends on FPGA, which can be utilized for a working with any number of floors, with the predetermined sources of info and yields. This controller can be executed for a lift with the required number of floors by just changing a control variable in the HDL code. This approach depends on a calculation which decreases the measure of calculation required, by concentrating just on the pertinent guidelines that enhances the execution of the gathering of lift framework.

Keywords: *Elevator Control System; Verilog HDL; FPGA; Xilinx ISE Design Suite.*

1. Introduction

Electronics is a branch of science in which electrons plays a vital role and it deals control of energy electrically. These days' electronic devices play a major role in our life. With the advancement of technology electronics devices are becoming much smaller, flexible, efficient and easy to use. These electronic devices are capable of implementing various functions. These electronic devices have various properties and are helpful to man in day to day life. Moore's law stated that the transistors double in size every year. With the increase in number of the transistors the size of electronics device shrinks. With the decrease in size of devices and increase in number of transistors i.e. in the order of millions we have various issues in power, routing etc. Modern technologies use MEMS, NEMS technologies.

Elevator is machine which is located in buildings used to transport people or luggage in a building from one floor to a particular floor. Elevators use the principle of conversion of energy i.e. electrical energy is converted into mechanical energy and vice versa. Earlier lifts or elevators used to be driven by hands or by animals. With the advancement of technology elevator systems started using PLC logic and microcontrollers. Major drawback of these technologies was that there is less number of inputs and outputs. By the implementation of elevators using FPGA technology there is an improvement in various factors like flexibility, low cost, efficiency, security, improvement in operational speed and parallel processing i.e. processing of inputs and outputs simultaneously. Major advantage of using FPGA is that it can be configured easily unlike microprocessors, microcontrollers which are difficult to configure. PLC's are used in automation and industries but there are limited to use for various practical applications. They can be used in wide range of applications by implementing them with various FPGA algorithms.

State Machines are those devices whose output is not only based on the output from recent inputs but also from previous inputs. These are used to model variety of systems like sequential patterns in DNA and to indicate the levels of fuel, oxygen and condition of valves i.e. whether they are opened or closed in space craft, aero planes etc. The advantage of state machine is that they can be used to determine the behavior of the system based on the control variable. Finite state machine also called as FSM is a device which contains the information about the set of states and the control variables. These are classified into two types Mealy State Machine and Moore State machine. In Mealy state machine present state depends upon both present state outputs and previous state outputs where as in case of Moore state machine present state depends only on recent input. State encoding is a process of assigning a value to each state. There are various techniques for State encoding. One hot encoding is a technique in which a state a can be determined based on the position of '1' bit. The advantage of this technique is that state decoding is simple. It can be used in flip flop rich architectures and in applications where fan-in is limited. The major drawback is that we have more usage of flip flop for each state and the width of combinational logic is reduced. Another type of encoding technique is binary encoding technique. In this type of technique states are assigned in binary sequence starting from binary '0' and so on. Numbers of flip flops are equivalent to the numbers of state variables. The major advantage is it uses less number of flip flops as a result number of state variables used to encode state machine are also less. The drawback is since the width of combinational logic is high; more combinational logic is used to decode each state. Gray encoding technique is similar to binary encoding technique and complexity of decoding logic is high.

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In our project elevator control system is a Mealy Finite state machine and the type of state encoding used is Binary encoding technique. Each floor is assigned with a state variable. Based on the control inputs elevator switches between floors. We implemented our project for three floors using Verilog which is implemented on Xilinx ISE Design suite 14.2. Verilog is a hardware description language which is used in the modelling of electronic systems. It is used to design and verify the digital circuit at Register Transfer Level of abstraction and it is a case sensitive language whose syntax is similar to that of C Programming. It contains hierarchy of modules and the communication between the modules is done based on the inputs, outputs and bidirectional ports. We have various control variables to determine the movement of lift i.e. whether lift is moving upwards or downwards or in the same floor. When there is no input applied lift remains in the ground floor. This can be helpful at time of emergencies or power failures because lift resumes to ground floor when there is no control input.

2. Algorithms

We have divided the proposed ECSS into different modules

a) Elevator Starting Module

In Elevator starting module , as the elevator start , ",EIDENTIY is a control signal which is used to determine whether lift is moving upward or downward or lift is present in the floor their we use the concept of Mealy State Machine. Each state is assigned a value based on binary state encoding technique. We have one input, one output and six control signals. These signals are Floor as input, Next floor as output, B1, B2, B3, S1, S2, S3 are control signals which are used to indicate the movement of elevator. If", EIDENTIFY ='00' lift is present in the floor, if", EIDENTFIY ="01" elevator moves upwards, if", EIDENTIFY ="10" lift moves downwards. Based on these signals elevator moves between various floors.

b) Elevator working module

In the IECFSM work in main work on the melay state machine. The following state table will show the working of Elevator Control.

S.NO	FLOOR	B1	B2	B3	S1	S2	S3	EIDENTIFY	NEXT FLOOR
1	0000001	1	0	0	0	0	0	00	0000001
2	0000001	0	1	0	0	1	0	01	0000010
3	0000001	0	0	1	0	0	1	01	0000011
4	0000010	0	1	0	0	0	0	00	0000010
5	0000010	0	0	1	0	0	1	01	0000011
6	0000010	1	0	0	1	0	0	10	0000001
7	0000011	0	0	1	0	0	0	00	0000011
8	0000011	0	1	0	0	1	0	10	0000010

Fig. 1: State Table.

If Floor is "0000001" and control signal B1 is "1" lift is present in floor 1.If Floor is "0000001" and control signal B2 is "1",S2 is "1", ",EIDENTIFY is "01" lift is moving from floor 1 to floor 2.If Floor is "0000001" and control signal B3 is "1",S3 is "1", ",EIDENTIFY is "01" lift is moving from floor 1 to floor 3.If Floor is "0000010" and control signal B2 is"1" lift is present in floor 2.If Floor is "0000010" and control signal B3 is "1",S3 is "1",EIDENTIFY is "01" lift is moving from floor 2 to floor 3.If Floor is "0000010" and control signal B1 is "1",S1 is "1", ",EIDENTIFY is "10" lift is moving from floor 2 to floor 1.If Floor is "0000011" and control signal B3 is"1" lift is present in floor 3.If Floor is "0000011" and control signal B2 is "1",S2 is "1", ",EIDENTIFY is "10" lift is moving from floor 3 to floor 2.

3. Designs and Implementation

In the design section the most significant was to outline the algorithm. Simplest possible algorithm was adopted fig.1. State Diagram for Elevator control where the elevator start working .According to the mealy state table EIDENTIFY – Control variable used to represent whether lift is present in floor or upwards or downwardsB1, B2, B3-Control variables used to represent the direction of the movement of the lift.S1, S2, S3-Control variables used to represent the direction of the movement of the lift.

Design rules are the following

- The following are the obtained results from the state table so that we can determine movement of elevator.
- In case of figure 1 it indicates that lift is present at Floor 1 as B1 is"1".
- In case of figure 2 it indicates that elevator is moving from Floor 1 to Floor 2 as B2 is"1",S2 is"1", EIDENTIFY is"01"
- In case of figure 3 it indicates that elevator is moving from Floor 1 to Floor 3 as B3 is"1",S3 is"1", EIDENTIFY is"01"
- In case of figure 4 it indicates that elevator is at Floor 2 as B2 is"1".
- In case of figure 5 it indicates that elevator is moving from Floor 2 to Floor 3 as B3 is"1",S3 is"1", ",EIDENTIFY is"01".
- In case of figure 6 it indicates that elevator is moving from Floor 2 to Floor 1 as B1 is"1",S1 is"1", ",EIDENTIFY is"10"
- In case of figure 7 it indicates that elevator is at Floor 3 as B3 is"1.
- In case of figure 8 it indicates that elevator is moving from Floor 3 to Floor 2 as B2 is"1",S2 is"1", EIDENTIFY is"10".

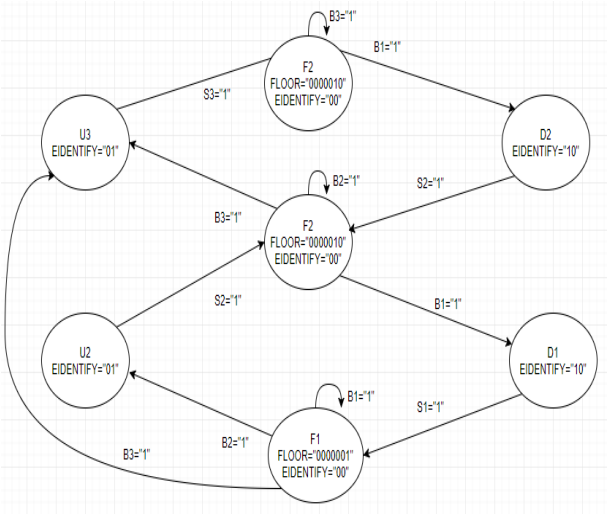


Fig. 2: State Diagram.

4. Practical realization

a) Design statistics and cell usage

```
Design Statistics
# IOs                              : 22

Cell Usage :
# BELS                             : 19
#      GND                         : 1
#      LUT3                        : 7
#      LUT4                        : 10
#      MUXF5                       : 1
# IO Buffers                       : 22
#      IBUF                        : 15
#      OBUF                        : 7
```

b) Device utilization summary

```
Selected Device : 3s500efg320-4


Number of Slices:                         10  out of   4656     0%
Number of 4 input LUTs:                   17  out of   9312     0%
Number of IOs:                            22
Number of bonded IOBs:                    22  out of    232     9%
```

c) Macro statistics

```
Macro Statistics
# Comparators                                          : 6
 2-bit comparator lessequal                            : 3
 7-bit comparator lessequal                            : 3
```

d) Timing Detail

```
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 125 / 2
-------------------------------------------------------------------------
Delay:               13.740ns (Levels of Logic = 10)
  Source:            Floor<4> (PAD)
  Destination:       Nextfloor<0> (PAD)

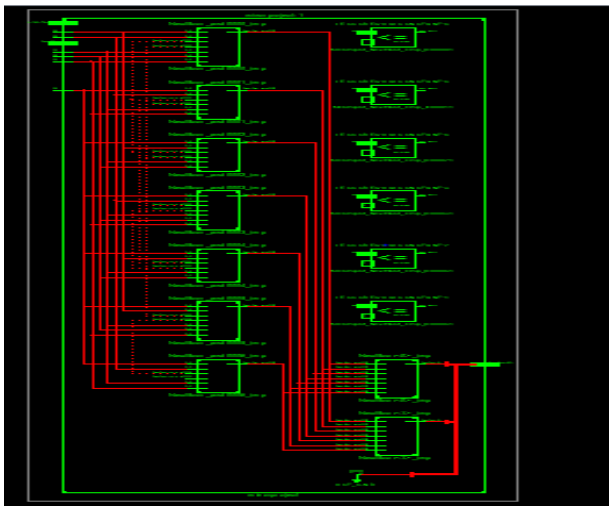
  Data Path: Floor<4> to Nextfloor<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.218   0.595  Floor_4_IBUF (Floor_4_IBUF)
     LUT3:I0->O            1   0.704   0.424  Nextfloor_and00001_SW0 (N14)
     LUT4:I3->O            2   0.704   0.622  Nextfloor_and00001 (N3)
     LUT4:I0->O            3   0.704   0.566  Nextfloor_and000321 (N4)
     LUT3:I2->O            2   0.704   0.526  Nextfloor_and0003_SW0 (N12)
     LUT4:I1->O            1   0.704   0.000  Nextfloor<0>59_G (N21)
     MUXF5:I1->O           1   0.321   0.424  Nextfloor<0>59 (Nextfloor<0>59)
     LUT4:I3->O            1   0.704   0.424  Nextfloor<0>89_SW0 (N16)
     LUT4:I3->O            1   0.704   0.420  Nextfloor<0>89 (Nextfloor_0_OBUF)
     OBUF:I->O                 3.272          Nextfloor_0_OBUF (Nextfloor<0>)
    ----------------------------------------
    Total                     13.740ns (9.739ns logic, 4.001ns route)
                                       (70.9% logic, 29.1% route)
```

```
Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 7.32 secs

-->

Total memory usage is 335956 kilobytes
```

e) RTL Schematic



5. Results

Elevator control is implemented using Verilog. We used the concept of Mealy state machine and Binary Encoding technique to encode various floors as states. We assigned some input variables, output variables and control variables. Based on the control variables elevator switches between the floors. This type of implementation is very flexible to implement because FPGA can be configured easily. We can simply change the number of floors or functionality of elevator simply by making minor changes in the program. This type of implementation requires less space for the hardware which is used to control the elevator system with a very less power consumption.

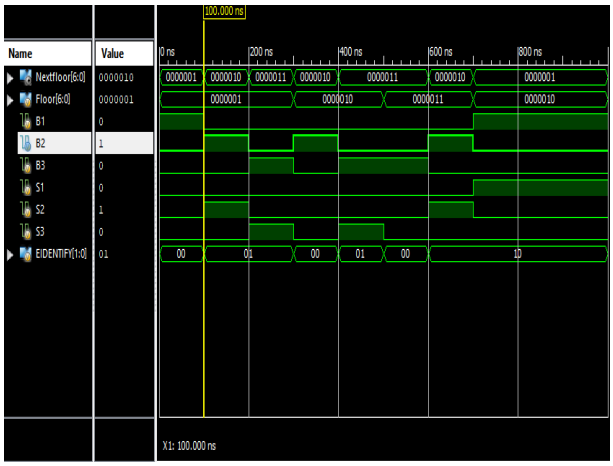


Fig. 3: Elevator at Floor 1 Elevator at Floor 1.

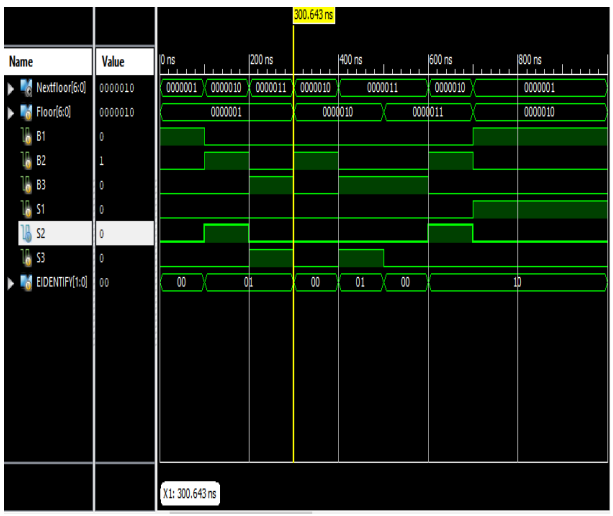


Fig. 4: Elevator Moving from Floor 1 to Floor 2.



Fig. 5: Elevator Moving From Floor 1 to Floor 3.

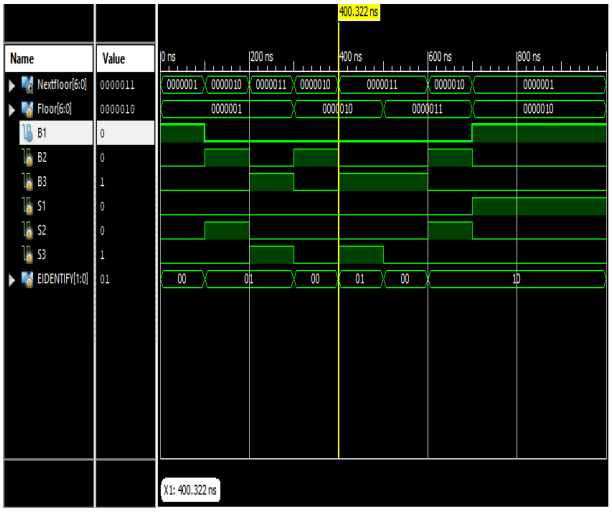


Fig. 6: Elevator at Floor 2.

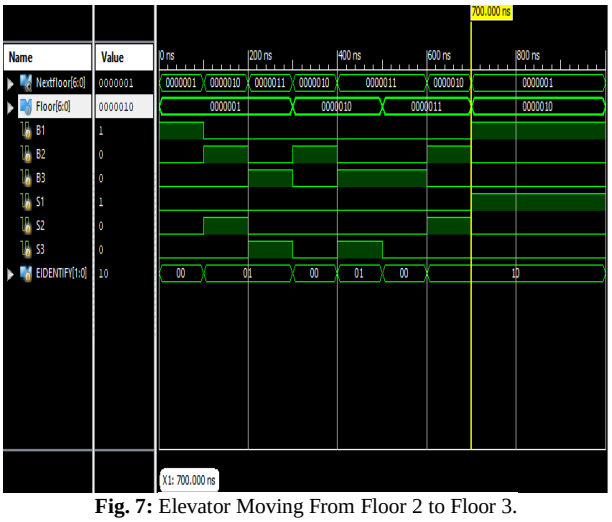


Fig. 7: Elevator Moving From Floor 2 to Floor 3.



Fig. 8: Elevator Moving from Floor 2 to Floor 1.

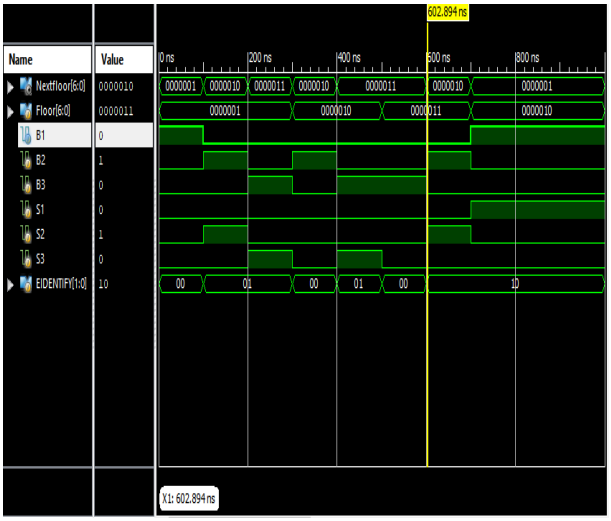


Fig. 9: Elevator at Floor 3.



Fig. 10: Elevator Moving from Floor 3 to Floor 2.

6. Conclusions

The FPGA based lift control framework gives greater adaptability, good than Microcontroller PLC based control system in which written by hand writing computer programs is utilized. Thus embedded system designer can plan a control system after a ton of process and mistakes that are comes in manually written HDL programming. The planned lift control system is executed utilizing finite state machine implementation utilizing Xilinx State CAD tools that enables designer to change system without content situated and blunders inclined principles in an efficient way. Simula-

tions have demonstrated that this strategy is very encouraging. Reconfiguration capability of FPGA based control system by programming is very fast because of parallel processing and this enhances productivity and reduces system development cost.

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