International Journal of Engineering & Technology, 7 (2.8) (2018) 56-62

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research Paper

Crosstalk noise minimization in novel through silicon via structures

K. Nageswara Rao [1] *, G. Veerendra Nath [1], K. Hari Kishore [2]

[1] Assistant Professor, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India-522502
[2] Professor, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India-522502
**Corresponding author E-mail: nagesh@kluniversity.in*

Abstract

In recent trends, through silicon via (TSV) is essential Technologies for 3-D IC integration because of its short interconnects length and high interconnect density. Beyond the existing structure of TSV, this paper provides a novel structure to investigate the crosstalk effect and same is simulated by using a SPICE simulator and 3-D field solver. The structure of the TSV comprises of copper surrounding by insulating liner, and silicon substrate. In existing structures, silicon dioxide (Sio_2) is used as insulating liner because of its material compatibility with silicon substrate. Several researches provide the problem of using Sio_2 is due to its high dielectric constant; as a consequence delay will increase. Therefore, Sio_2 is not appropriate for high performance applications. In this work, a novel TSV structure is reported to improve the TSV performance which uses poly-propylene polymer liner instead of oxide liner. Signal TSV is enclosed by using a poly-propylene liner and amid the analysis with doping region is created around the ground TSV. For comparison purposes, conventional and proposed TSV structures are simulated. The proposed TSV's structure simulation results in 30% decrease in crosstalk over existing TSV structures.

Keywords: *Through Silicon via (TSV); Poly-Propylene Liner; Polymer Capacitance; Depletion Capacitance; Crosstalk.*

1. Introduction

In recent days, through silicon via (TSV) interconnects are playing a major role in 3-D IC integration. The advantages of TSV interconnects are low power consumption, smaller form factor, better performance, and higher functional density. TSVs are the vertical interconnects used to enable the vertical stacking of Integrated circuit (IC) chips. The structure of the TSV [1] composed of Cu surrounded with insulating liner and silicon substrate. The usage of insulating liner is to avoid the signal leakage from the metal (Cu) to silicon substrate. In the traditional TSV structures, silicon di- oxide (Sio_2) is used as insulating liner [2] because of its material compatibility with the silicon substrate. Sio_2 liner has small thickness which is roughly equivalent to 0.01µm and it has large dielectric constant which is approximately equal to 3.9. Because of high dielectric constant, Sio_2 liner develops a large insulating capacitance which impacts on degradation of TSV performance [3]. Hence, Sio_2 liner is not appropriate for high performance applications. In addition to that few authors were provided the problems of Sio_2 liner. They accounted the problem of deposition of uniform thin layer on the sidewalls of deep reactive ion etching (DRIE) etched vias. Because of the inherent scallops on the sidewalls of TSVs, stress concentration at the scallop edges brings about failure of ultra-thin barrier layers, current spillage and deterioration of electrical performance. To enhance the TSV performance and mitigate the insulating capacitance, low dielectric constant liners are used instead of Sio_2 liners.

In general, polymer liner has low dielectric constant, elastic modulus and large thickness. Due to the low dielectric constant of polymer, it develops a less insulating capacitance between metal and silicon substrate that results in decreasing of delay. Hence, polymer liners are well appropriate for high performance applications. Additionally, Current spillage is avoided by eliminating the discontinuity of barriers using a large and uniform thickness of polymer liners. Moreover, due to low elastic modulus, polymer liner can also act as a barrier layer in between the silicon substrate and metal to avoid the thermal stresses. In the proposed model, a novel TSV structure is constructed with polypropylene polymer liner as insulating liner.

The TSVs with polymer liners to be fabricated with a completely different method [4] which is contrasting to TSVs with silicon dioxide layers deposited by plasma-enhanced chemical vapor deposition (PECVD). It is possible to fill polymer into a narrow trench using spin-coating or dispensing techniques. Instead of using circular vias hollow-cylinder polymer is completely filled by using annular trenches and coated thin polymer layers. The large and uniform thickness polymer liners surrounding to Cu metal is possible with the annular trench based fabrication.

The rest of the paper is organized as follows: The electrical modeling of TSV with analytical equations is reported in section 2. The results and discussions based on the parameter variations of TSV is reported in section 3. Finally, section 4 concludes the work.

Copyright © 2018 K. Nageswara Rao et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

2. Electrical modeling of TSV with analytic equations

The proposed TSV structure comprises of three cylindrical signal-ground-signal pattern with height 100 µm and radius 10 µm as shown in Fig. 1. The first and third cylinder is designed with copper surrounded by polypropylene liner thickness 0.1 µm and heavily doped silicon MOS depletion layer width 0.68 µm. The middle cylinder is designed with copper and surrounded by doping layer thickness 0.1 µm. The dielectric constant (ε_r) of poly-propylene liner, Sio_2, silicon, copper is 2.3, 3.9, 11.9 and 1.0, respectively.

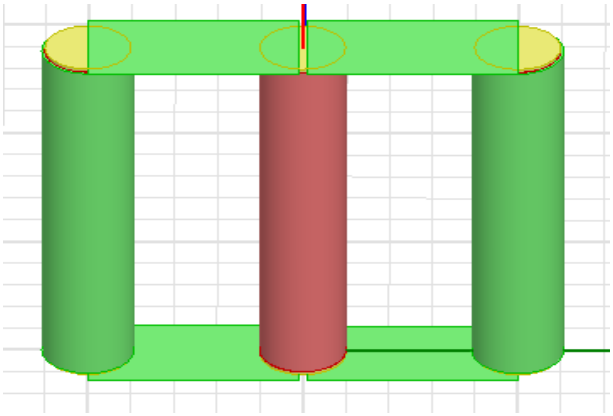


Fig. 1: Signal-Ground-Signal Pattern for the Proposed TSV Structure.

In this section, analytic RLGC components of the proposed equivalent circuit model of a TSV are proposed and electrically modeled with analytic equations which are functions of material properties, structural parameters, frequency, and etc. The proposed equivalent circuit model Fig. 2 is acquired based on the physical structure of a TSV. Among various TSV parasitic, the capacitance of a TSV is the most vital component which governs the overall electrical behavior of a TSV.

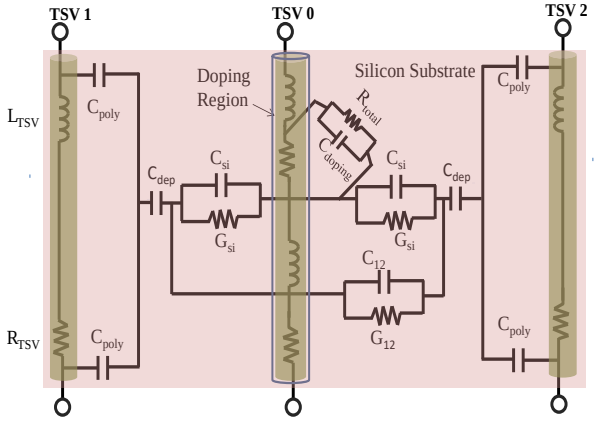
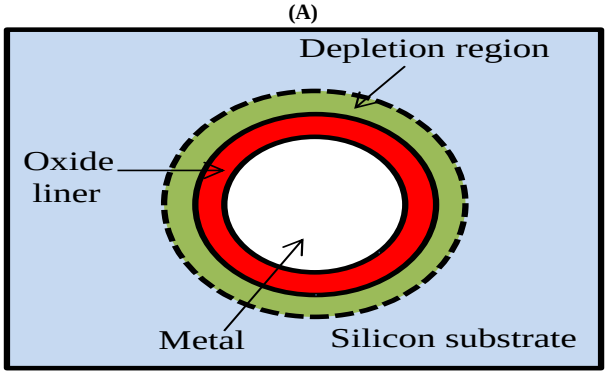
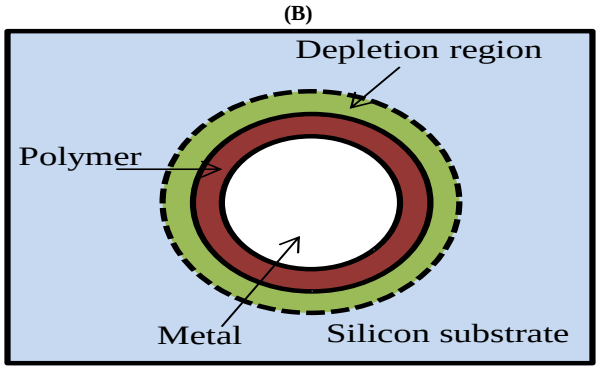


Fig. 2: Electrical Equivalent Model for the Novel TSV Structure.





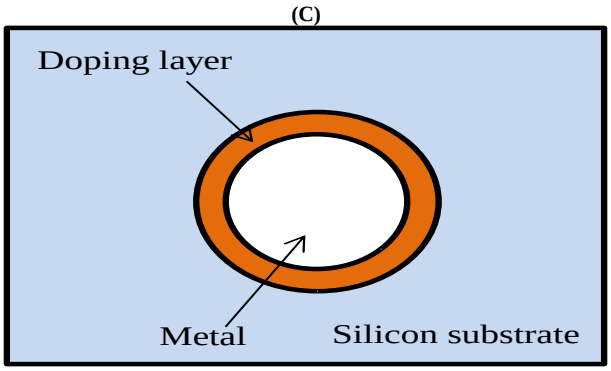


Fig. 3: (A) Top View of the Conventional TSV Structure that Uses Oxide Liner (B) Top View of Proposed Signal TSV Structure that Uses Polymer Liner (C) Top View of the Proposed Ground TSV Structure.

Each of the RLGC components corresponds to a structure of a TSV. The analytic RLGC equations are derived from the physical structure with the design parameters [5], [6]. Therefore, each RLGC equation is a function of the variables from the design parameters. The resistance and inductance of the TSV is analytically modeled as in (1) and (2), respectively.

$$R_{TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times \left(\frac{d_{TSV}}{2}\right)^2} \tag{1}$$

$$L_{TSV} = \frac{1}{2}\left\{\frac{\mu_0 \mu_{r,TSV}}{2\pi} \times h_{TSV} \times \ln\left(\frac{\rho_{TSV}}{r_{TSV}}\right)\right\} \tag{2}$$

Where hTSV, dTSV, rTSV are the length, diameter, radius of the TSV.

The TSV is surrounded by insulating liner to separate it from the conductive silicon substrate. Due to this insulation layer, there is an insulator capacitance represented by $C_{polymer}$. The depletion capacitance is also considered in series to the polymer capacitance because the substrate is fully biased to the ground [7], [8]. The polymer capacitance and depletion capacitance can be calculated as

$$C_{polymer} = \frac{1}{2}\left\{2\pi \times \varepsilon_0 \varepsilon_{r,polymer} \times \frac{h_{TSV}}{\ln\left(\frac{r_{TSV} + t_{poly}}{r_{TSV}}\right)}\right\} \tag{3}$$

$$C_{dep} = \frac{\varepsilon_{Si} h_{TSV}}{\ln\left(1+\frac{w_{dep}}{r_0}\right)} \tag{4}$$

The metal-silicon contact depends on the metal used for the TSV and silicon substrate dopant density. An ohmic contact and Schottky contact can be formed depends on the doping concentration of silicon. The ohmic contact is a less resistance junction and it can be formed for highly doped silicon. Preferably, the metal-silicon contact resistance must be low. The metal-silicon contact resistance increases, when lower doping concentrations are used. Therefore, the contact resistance needs to be taken into account. The contact resistance and doping region resistance both contribute to give the total resistance.

$$R_{Total} = \frac{1}{2\pi h_{TSV}} \ln\frac{r_0+t}{r_0} \cdot \frac{1}{\sigma_{eq}} \tag{5}$$

Since the doping region contains dielectric, it is needed to consider the doping capacitance. It is calculated as

$$C_{doping} = \frac{\varepsilon_{Si} h_{TSV}}{\ln\left(1+\frac{r}{t_0}\right)} \tag{6}$$

We considered the ground TSV as the reference ground, the unit-length and mutual-inductances of signal TSV can be evaluated as

$$L_{ij} = \frac{\mu_0}{2\pi} \ln\left(\frac{l_{i0}^2}{R_i R_0}\right), (i = j) \tag{7a}$$

$$L_{ij} = \frac{\mu_0}{2\pi} \ln\left(\frac{l_{i0} l_{j0}}{R_0 l_{ij}}\right), (i \neq j) \quad (i, j = 1,2) \tag{7b}$$

The coupled capacitance and inductance, C12 and G12 between signal TSVs can be obtained from the following 2×2 C and G matrix as

$$C = \mu_0 \varepsilon_{Si} h_{TSV} L^{-1}, \quad G = \mu_0 \sigma_{Si} h_{TSV} L^{-1} \tag{8}$$

Where ε_{Si} and σ_{Si} are the dielectric constant and conductivity of silicon substrate and h_T is the TSV height. There is a capacitance and conductance between the signal and ground TSVs because silicon is a semiconductor [9]. $C_{Si\text{-}Sub}$ is expressed as a function of d_{TSV}, p_{TSV}, and h_T. The h_T term indicates the height where the electric fields are formed between the signal and ground TSVs in the silicon substrate. The relative permittivity of the silicon substrate, $e_{r,si}$ is additionally a variable of $C_{Si\text{-}sub}$.

$$C_{Si-Sub} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,Si}}{\cosh^{-1}\left(\frac{\rho_{TSV}}{d_{TSV}}\right)} \times h_T \tag{9}$$

The physical origin of the G_{SiSub} is the silicon conductivity, σ_{Si}, which is determined by the majority carrier concentration. Therefore, G_{SiSub} is expressed as

$$G_{Si-Sub} = \frac{\pi \times \sigma_{Si}}{\cosh^{-1}\left(\frac{\rho_{TSV}}{d_{TSV}}\right)} \times h_T \tag{10}$$

3. Results and discussion

In this section, it is considered that TSV radius, length, and the thickness of the polymer liner are 10 µm, 100 µm, and 0.1 µm. The pitch between TSVs is 50 µm. The silicon conductivity (σ_{Si}) is 10 S/m, and ground doping conductivity is 0.1 S/m. For comparison purposes, the conventional TSV structure is also simulated which uses silicon dioxide liner. The calculated MOS depletion region is 0.68 µm for the signal TSV with signal excitation of 0-1 V. The depletion region around the ground TSV in conventional structure is 0.28 µm.

The performance of a novel TSV structure is analyzed by varying different parameters like TSV radius, height, and thickness of the polymer liner. For comparison purposes, conventional TSV structure is simulated using SPICE software. The proposed TSV structure simulation results reduce the crosstalk dramatically compared to the conventional TSV structure.

Among various parameters like r_{TSV}, h_{TSV}, and t_{poly} the thickness of the polymer liner is changed and rest of the parameters kept constant. For comparison purposes, the conventional TSV structure is also simulated, shown in Fig. 4. The proposed TSV structure reduces the crosstalk because the polymer capacitance is less compared to oxide capacitance.

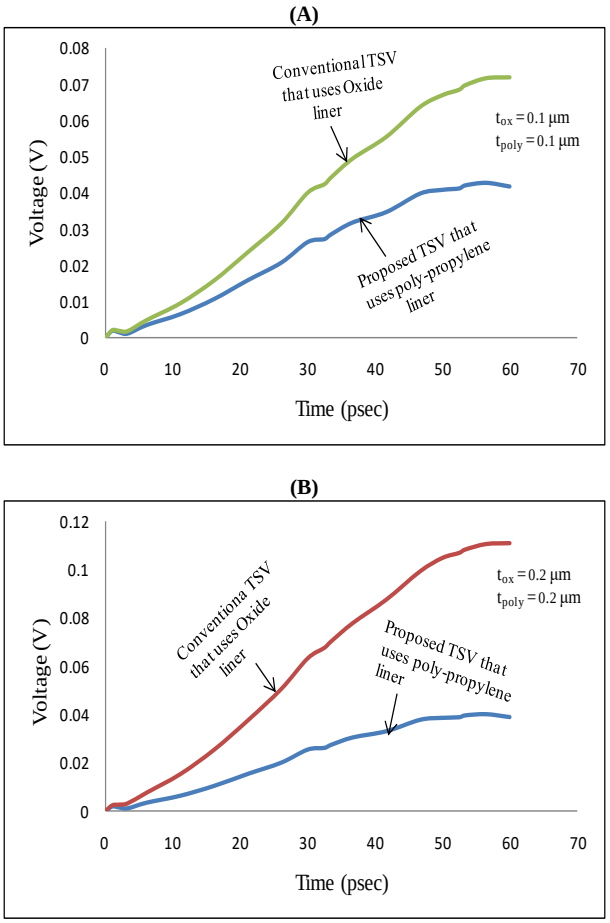


Fig. 4: Comparison of Proposed TSV Structure Simulation with the Conventional TSV Structure with Thickness Variation. (A) T_{ox}, T_{poly} = 0.1 µm (B) T_{ox}, T_{poly} = 0.2 µm.

The thickness for both oxide liner and poly-propylene insulating liner is changed, impact of changing the thickness will result in varying of insulating capacitance. The oxide capacitance is more compared to polymer capacitance because of its high dielectric

constant. Due to the reduction in polymer capacitance it leads to decrease in the crosstalk effect. Therefore, the crosstalk in proposed TSV structure is decreased nearly 25% compared to conventional TSV structure.

Similarly, the conventional and proposed TSV structure is validated with r_{TSV} variation as shown in Fig. 5.

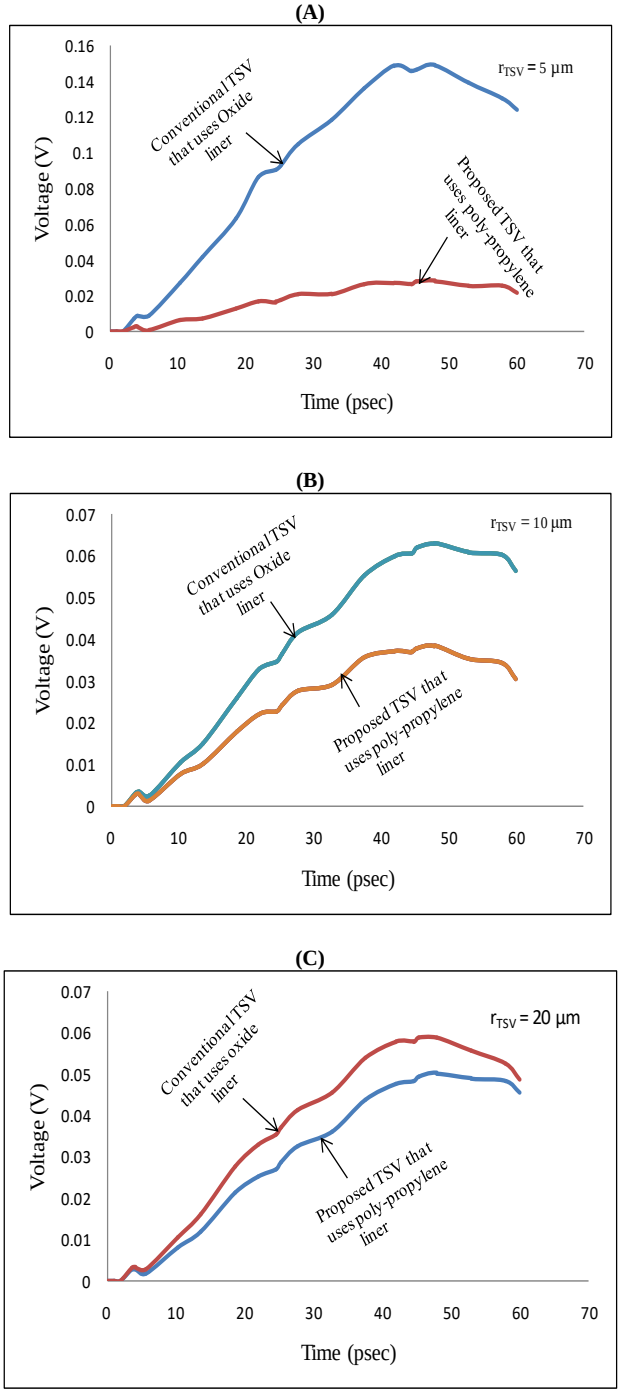


Fig. 5: Comparison of Proposed TSV Structure Simulation with the Conventional TSV Structure with R_{tsv} Variation. (A) R_{tsv} = 10 µm (B) R_{tsv} = 5 µm (C) R_{tsv} = 20 µm.

Impact of changing the radius of TSV (r_{TSV}) will result in varying of insulating capacitance. Changing of r_{TSV} will also effect in the depletion capacitance, doping capacitance of signal and ground TSV. In conventional TSV structure, there is depletion capacitance also for ground TSV. On the other hand, doping capacitance for the ground TSV is considered in proposed TSV structure. Compared to depletion capacitance, doping capacitance for ground TSV is negligibly small. Therefore, the crosstalk is reduced in proposed TSV structure. The proposed and conventional TSV structure with h_T variation is also validated as shown in Fig. 6.

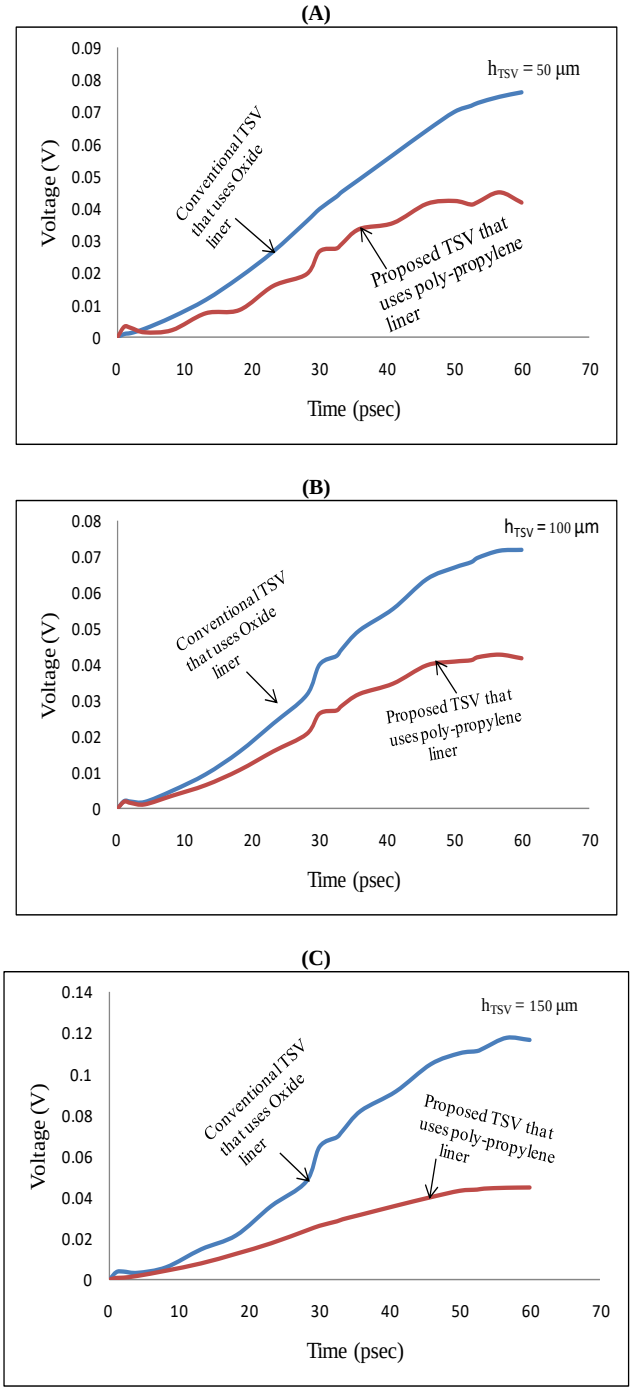


Fig. 6: Comparison of Proposed TSV Structure Simulation with the Conventional TSV Structure with H_{tsv} Variation (A) H_{tsv}= 100 µm (B) H_{tsv} = 50 µm (C) H_{tsv} = 150 µm.

Further, it is observed that the TSV parasitic like resistance, inductance, and capacitance are changing with respect to design parameters of TSV like h_{TSV} and r_{TSV}. For comparison purposes conventional TSV structure is also simulated. For both conventional and proposed TSV structures, variation in resistance and inductance is same. The only varying parameter is capacitance because of difference in dielectric constant of oxide and poly-propylene polymer liners.

The capacitance value is gradually decreasing in proposed TSV structure compared to conventional TSV structure is shown in Fig. 7.

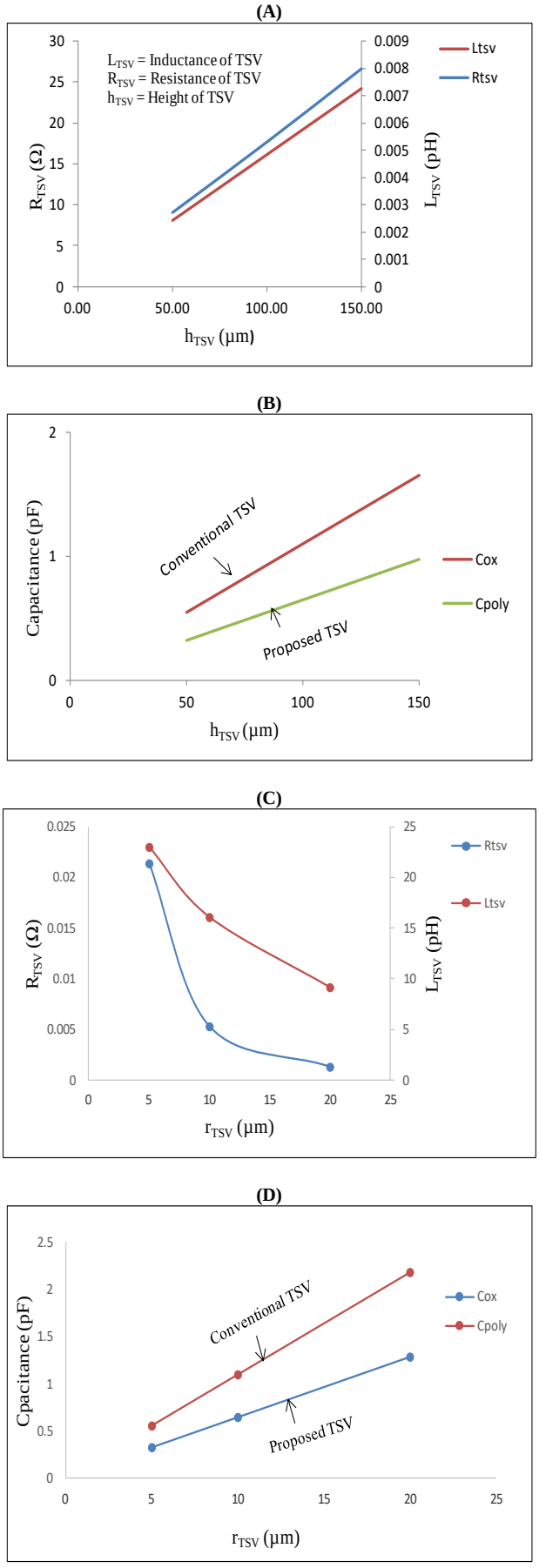
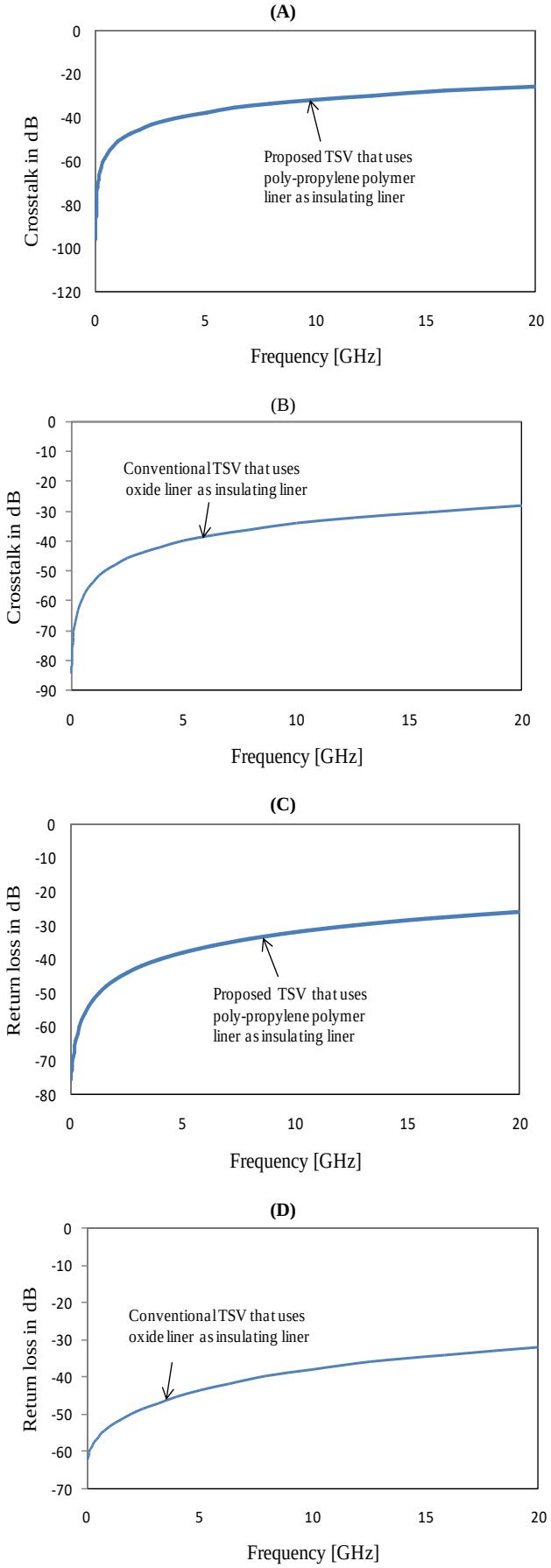


Fig. 7: Variation In R, L, C Parasitic with Respect to Design Parameters of TSV (A) Resistance and Inductance with Respect to H_{tsv} for Both Conventional and Proposed TSV Structure (B) Capacitance with Respect to H_{tsv} for Conventional and Proposed TSV Structure (C) Resistance and Inductance with Respect to R_{tsv} for Both Conventional and Proposed TSV Structure (D) Capacitance with Respect to R_{tsv} for Conventional and Proposed TSV Structure.

In addition to that the proposed TSV structure is simulated with 3-D field solver, HFSS of a soft. Among many design parameters r_{TSV}, h_{TSV} and ρ_{TSV} are swept to validate the proposed TSV structure up to 20 GHz. The results obtained with this a soft HFSS simulation tool are shown in Fig. 7.



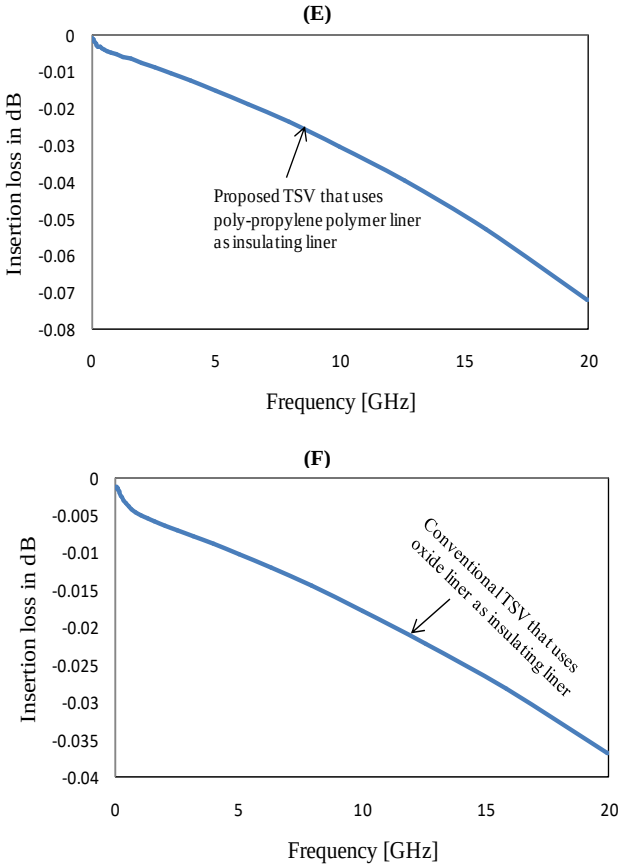


Fig. 8: Simulation Results of Proposed TSV Structure Using 3-D Field Solver.

From Fig. 8, the crosstalk, return loss, and insertion loss in the proposed TSV structure is presented. Fig. 8(a) & 8(b) shows the crosstalk comparison for both conventional and proposed TSV structure. The crosstalk could be decreased in proposed TSV structure because of poly-propylene polymer liner is used. In the proposed TSV structure, reduction in crosstalk was observed which is nearly equal to 15%. Fig. 8(c) & 8(d) shows the return loss in proposed and conventional TSV structure. The results dedicates that return loss will be less in proposed TSV structure compared to traditional TSV structure. Fig. 8(e) & 8(f) shows the insertion loss in proposed and conventional TSV structures.

4. Conclusion

A novel TSV structure is proposed to investigate crosstalk effect induced in TSVs. The proposed TSV structure that uses poly-propylene polymer liner as insulating liner because of its low dielectric constant. This work contribute to analyze the impact of insulating capacitance on crosstalk noise. Impact of changing the parameters like TSV radius, height and oxide liner thickness on crosstalk is studied. By changing the design parameters how the crossatlk will be decreased in proposed TSV structure was observed. For comparson purposes, the conventional TSV structure is also simulated. The proposed TSV modelling results shows nearly 30% decrease in crosstalk compared to conventional TSV structures. The proposed TSV structure was also simulated by using 3-D field solver and compared with conventional TSV structures. From these simulation results, crosstalk in proposed TSV structure could be decreased nearly equal to 15% and leading to better perforrmance.

References

[1] T. Bandhopadhyay, K. J. Han, and D. Chung, “Rigorous electrical modeling of Through Silicon Vias (TSVs) with MOS capacitance effects,” IEEE Trans. Comp. Packag. Manufact. Technol., vol. 1, pp. 893–903, 2011. https://doi.org/10.1109/TCPMT.2011.2120607.

[2] DC Yang, J. Xie, and M. Swaminathan, “A Rigorous Model for Through-Silicon Vias with Ohmic Contact in Silicon Interposer,” IEEE microwave and wireless components letters, 2013. https://doi.org/10.1109/LMWC.2013.2270459.

[3] Yoon, K., G. Kim, W. Lee, T. Song, and J. Kim, L.Qian, Y.xia, and G.Liang , “ Study on crosstalk characteristic of carbon nanotube through silicon vias for three dimensional integration,” in Microelectronics journal, Vol. 46, pp. 572-580, jul.2015.

[4] C. Huang, Q. Chen, and Z. Wang, “Polymer liner formation in TSVs for 3-D integration,” IEEE Trans. Comp. Packag. Manufact. Technol., vol. 3, no. 7, July 2013.

[5] J. Kim, J. S. Pak, and J. Cho, “High-frequency scalable electrical model and analysis of a through silicon via (TSV),” IEEE Trans. Comp. Packag. Manufact. Technol., vol. 1, no. 2, pp. 181–195, 2011. https://doi.org/10.1109/TCPMT.2010.2101890.

[6] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, “Electrical modeling and characterization of through silicon via for three-dimensional ICs,” IEEE Trans. Electron Devices, vol. 57, pp. 256–262, 2010. https://doi.org/10.1109/TED.2009.2034508.

[7] X. Wang, M. Xiong, and Z. Chen, “Wideband Capacitance Evaluation of Silicon-Insulator-Silicon Through-Silicon-Vias for 3D Integration Applications,” IEEE Electron Device Letters, vol. 37, no. 2, Feb. 2016. https://doi.org/10.1109/LED.2015.2506551.

[8] A. E. Engin and N. S. Raghavan, “Metal semiconductor (MES) TSVs in 3D ICs: Electrical modeling and design,” in Proc. IEEE Int. 3D Syst. Integr. Conf., Japan, pp. 1–4, 2012. https://doi.org/10.1109/3DIC.2012.6263049.

[9] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, “ Electrical modeling and characterization of through silicon via for three-dimensional ICs,” IEEE Trans. Electron Devices, Vol. 57, no. 1, pp. 256-262, Jan. 2010. https://doi.org/10.1109/TED.2009.2034508.

[10] Dr. Seetaiah Kilaru, Hari Kishore K, Sravani T, Anvesh Chowdary L, Balaji T “Review and Analysis of Promising Technologies with Respect to fifth Generation Networks”, 2014 First International Conference on Networks & Soft Computing, ISSN:978-1-4799-3486-7/14,pp.270-273,August2014.

[11] Meka Bharadwaj, Hari Kishore "Enhanced Launch-Off-Capture Testing Using BIST Designs” Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.12, Issue No.3, page: 636-643, April 2017.

[12] P Bala Gopal, K Hari Kishore, B.Praveen Kittu “An FPGA Implementation of On Chip UART Testing with BIST Techniques”, International Journal of Applied Engineering Research, ISSN 0973-4562, Volume 10, Number 14 , pp. 34047-34051, August 2015.

[13] A Murali, K Hari Kishore, D Venkat Reddy "Integrating FPGAs with Trigger Circuitry Core System Insertions for Observability in Debugging Process” Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.11, Issue No.12, page: 2643-2650, December 2016.

[14] Mahesh Mudavath, K Hari Kishore, D Venkat Reddy "Design of CMOS RF Front-End of Low Noise Amplifier for LTE System Applications Integrating FPGAs” Asian Journal of Information Technology, ISSN No: 1682-3915, Vol No.15, Issue No.20, page: 4040-4047, December 2016.

[15] N Bala Dastagiri, K Hari Kishore "Novel Design of Low Power Latch Comparator in 45nm for Cardiac Signal Monitoring”, International Journal of Control Theory and Applications, ISSN No: 0974-5572, Vol No.9, Issue No.49, page: 117-123, May 2016.

[16] N Bala Gopal, Kakarla Hari Kishore "Reduction of Kickback Noise in Latched Comparators for Cardiac IMDs” Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.43, Page: 1-6, November 2016.

[17] S Nazeer Hussain, K Hari Kishore "Computational Optimization of Placement and Routing using Genetic Algorithm” Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.47, page: 1-4, December 2016.

[18] N.Prathima, K.Hari Kishore, “Design of a Low Power and High Performance Digital Multiplier Using a Novel 8T Adder”, International Journal of Engineering Research and Applications, ISSN: 2248-9622, Vol. 3, Issue.1, Jan-Feb., 2013.

[19] Harikishore Kakarla, Madhavi Latha M and Habibulla Khan, “Transition Optimization in Fault Free Memory Application Using

Bus-Align Mode", European Journal of Scientific Research, Vol.112, No.2, pp.237-245, ISSN: 1450-216x135/1450-202x, October 2013.

[20] SHAIK.RAZIA, M.R.NARASINGARAO published "Machine learning techniques for thyroid disease diagnosis - A review" in Scopus Indexed Journal INDJST (Indian Journal of Science and Technology, ISSN: 09746846, volume-9, Issue 28, July 2016, Article number 93705).

[21] SHAIK.RAZIA, M.R.NARASINGARAO published "A Neuro computing frame work for thyroid disease diagnosis using machine learning techniques" in Scopus Indexed Journal JATIT (Journal of Theoretical and Applied Information Technology, 15th May 2017. Vol.95. No.9. Pages 1996-2005) ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195.

[22] T. Padmapriya and V. Saminadan, "Distributed Load Balancing for Multiuser Multi-class Traffic in MIMO LTE-Advanced Networks", Research Journal of Applied Sciences, Engineering and Technology (RJASET) - Maxwell Scientific Organization, ISSN: 2040-7459; e-ISSN: 2040-7467, vol.12, no.8, pp: 813-822, April 2016.

[23] S.V.Manikanthan and K.Baskaran "Low Cost VLSI Design Implementation of Sorting Network for ACSFD in Wireless Sensor Network", CiiT International Journal of Programmable Device Circuits and Systems,Print: ISSN 0974 – 973X & Online: ISSN 0974 – 9624, Issue : November 2011, PDCS112011008.