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Research Paper

A 14-bit 10kS/s power efficient 65nm SAR ADC for cardiac implantable medical devices

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Abstract

This brief presents a 10kS/s 14 bit 12.5 ENOB Successive Approximation Register Analog-to- Digital Converter for Cardiac Implantable Medical. For achieving power efficient operation, SAR ADC employ SAR control, a new power and noise efficient comparator topology, non- binary weighted capacitive DAC. The linearity of implemented SAR ADC is enhanced with the uniform geometry of non-binary weighted capacitive DAC.The proposed SAR ADC is implemented using 65nm CMOS technology. The latched comparator consumes a power of 2.4uW and it provides an ENOB of 12.6 at a supply voltage of 1V.The INL is between -2.7/+1.6 LSB and DNL is between -0.6/+1.4LSB. The FOM of ADC is 40fJ/conv. Step which is comparable with existing ADC topologies.

Keywords: *Successive Approximation Register Analog-to-Digital Converter; ENOB; INL; DNL; Cardiac Implantable Medical Device; Comparator.*

1. Introduction

The advancement in CMOS Technology has spurred increasing demand for integrated cardiac implantable medical devices like defibrillators and pacemakers. These implantable devices have to operate with a non-rechargeable battery over their life time almost for 10 years. Among various components available in the implantable devices, Analog-to-Digital Converters are power hungry and also the most critical component in measuring cardiac signals. Cardiac Signals are low frequency analog signals and doesn't require high speed for their conversion. Thus designing an ADC for cardiac applications with low power consumption and required conversion accuracy makes it a great challenge. Successive Approximation ADCs are being widely used in biomedical applications as they operate with low speed and medium resolution and also with low power budget. Also the main reason for utilizing SAR ADCs in cardiac Implantable devices is due to their simplicity in their structure. Normally SAR ADCs show very high energy efficiency, but due to comparator noise and capacitor mismatch, SAR ADCs are limited to medium resolution. To overcome the effect of capacitor mismatch, binary weighted capacitance array in DACs has been implemented in [1], [2]. An alternative technique called dithering has been proposed to cancel the errors in the DAC and also to improve the linearity [3], [4]. Many attempts have been made to cut down the power consumed by SAR ADC with the prominence on designing latched comparator and capacitive DAC. In this work, Low power SAR ADC is designed by modifying the existing architectures of latched comparator and effective capacitive DAC. The architecture of DAC is modified such that the size of capacitance in the DAC is reduced and in turn power consumption and area of DAC are also reduced. In this work, the implementation of non-binary weighted DAC is done. This type of converter exhibits redundancy during the conversion but however array capacitance value in the DAC is rounded off to the nearest integer value, such that it leads to uniform geometry. Moreover, the power consumption of latched comparator is also reduced by modifying its architecture, which indeed reduces the charge injection, kickback noise and clock feedthrough.
The organization of the brief is as follows. The architectural implementation of an ADC is discussed in section II. The simulation results of SAR ADC and its comparison is presented in section III followed by conclusion remarks in section IV.

2. Proposed architectural implementation of SAR-ADC

The architecture of SAR ADC implementing in cardiac IMDs is depicted in figure 1. It mainly consists of a synchronous SAR, latched dynamic comparator and a non-binary differential weighted capacitive DAC and. The differential inputs to the DAC are sampled on the capacitive array by using bootstrapped switches.

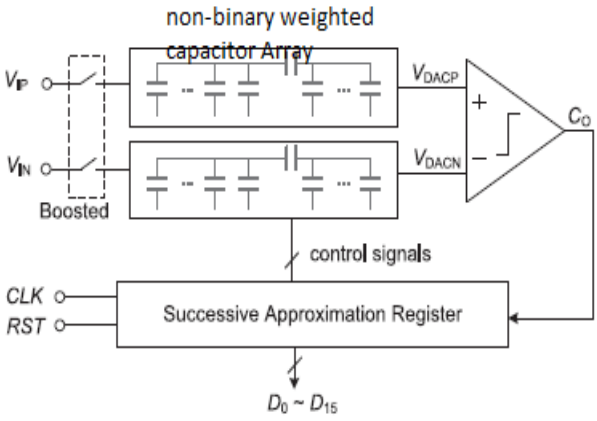


Fig. 1: Architecture of Proposed SAR ADC.

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a) Capacitive DAC

In order to achieve a 14 bits resolution, we have implemented a split array DAC consisting of 11 bits primary DAC and a secondary DAC of 5 bits along side of bridge capacitor. For achieving uniform geometry and good linearity, the implemented value of non-binary capacitive array is adjusted to the nearby integer value. After adjusting the value, the dynamic range of capacitive DAC has to be greater than 14 bits resolution. The capacitor in the capacitance array is implemented such that its density is high. The value of each capacitance is approximately 27fF where as total capacitance of sampling capacitance is about 30pF.The non binary weighted capacitive array is shown in figure 2.

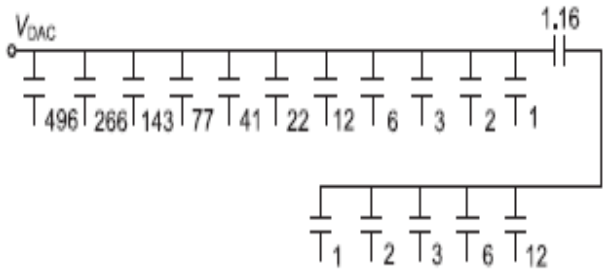


Fig. 2: Non-Binary Weighted Capacitance Array Rounded Off to Nearest Integer Value.

For a non –binary weighted capacitor array split DAC has radix k, the capacitors present at the bridge capacitor terminals also has the radix. Here primary plate of bridge capacitor is joined to secondary DAC, such that the linearity error occurred due to parasitic can be minimized. To enable the ADC for correcting under approximation and over approximation decision errors , it is required that the decision levels are shifted to middle of redundancy stage [6], [7].For shifting the level, an additional capacitor is used besides the main capacitance array [5].A new approach is introduced in which decision bit and lower weighted bit are switched simultaneously[8], [9].Once the decision is happened, lower order bit is turn downed to its original state. The secondary bit has a weight equal to the redundancy of decision bit. The position of Secondary bit is written as

$$W_j + \frac{1}{2} \cdot \left(\sum_{i=1}^{j-1} W_i - W_j \right) = W_j + W_{j-k}$$

Where k is denoted as distance between the decision and secondary bits and W_j is the weight of the decision bit [10].

b) Latched Comparator

In a latched comparator, apart from thermal noise, clock feedthrough ,comparator offset voltage, kickback noise; and charge injection are also the main sources of errors. In a SAR ADC, the offset in transfer curve can be corrected easily, therefore offset of the latched comparator can be easily tolerated. Moreover, the other sources of errors must be reduced. Using a few traditional techniques may reduce the errors but considerably increases power consumption [11], [12].

Kickback noise and clock feedthrough are produced at the edge of the latched comparator output signal and at the clock of the comparator respectively. In case of cardiac applications, the latched comparator has low clock frequency and hence the latched comparator has ample time for making its decisions. Therefore kickback noise and clock feedthrough can be reduced by increasing raise time and fall time of comparator clock and its output signal.

The architecture of proposed comparator is depicted in the figure 3.When the latched comparator is reset state, both the outputs of the dynamic latched are pulled to VDD. As the transistors M9 and M10 are in OFF state, they isolate the inputs from being connected to output. During the comparison phase the outputs are pulled to VDD and GND depending on the inputs applied.If INP>INN, the corresponding output OUTP tends to discharge to ground faster than OUTN through the transistors M13 and M14.The transistors M11 and M12 are connected in a fashion such that the charge injection and clock feedthrough is reduced. Due to the isolation transistors M9 and M10 the outputs doesn't have any effect on the inputs of the comparator during the transition of the latch.

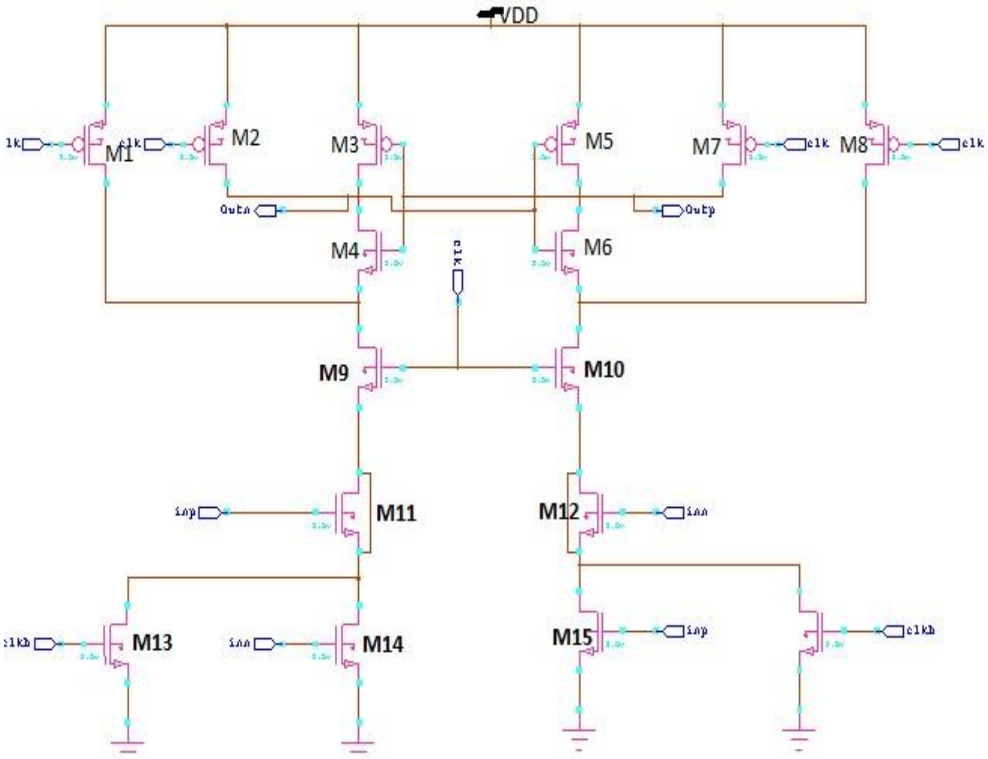


Fig. 3: Architecture of Proposed Latched Comparator to Minimize Kickback Noise and Clock Feedthrough.

From the figure 4, it is seen that the conventional latched comparator suffers from more kickback noise(glitches can be seen) when compared with proposed architecture. In the proposed architecture, the common mode signal V_{CM} is kept above the threshold voltage that is in between mid rail voltages.

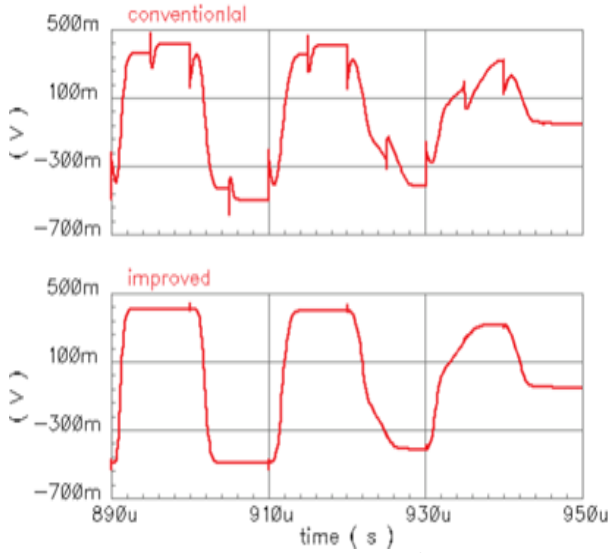


Fig.4: Transient Simulation Results of Latch Input.

c) Sar Digital Control Logic

SAR logic control is demonstrated in figure 5.It mainly consists of positive transparent latches, shift registers and a combinational logic switch. The latch is used to store the decisions taken by the comparator, combinational logic switch is used to generate the control signals required for differential DAC and shift register is used to generate pulses. In this work, to complete a single conversion we require a 17 clock cycles, 16 for bit decisions and remaining for sampling [13], [14].

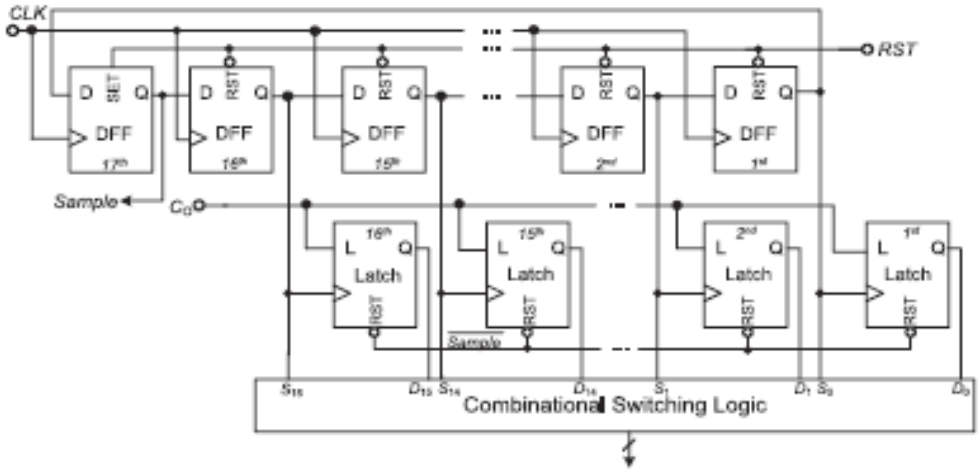


Fig. 5: Block Diagram of SAR Digital Control Logic.

3. Experimental results

In this work, the SAR ADC is implemented using 65nm CMOS technology. Also the proposed 10KS/s SAR ADC is measured at a supply voltage of 1V.The transient simulation result of SAR ADC is plotted in the figure 6.The static performance of an ADC is measured and depicted in Figure 7 .The peak Value of Differential Non Linearity error is +1.4/-0.6 LSB where as Peak value of Integrated Non Linearity error is +1.6/-2.7 LSB. The dynamic performance characteristics of SAR ADC is plotted in figure 8. The SNDR and SFDR are constant with a minimum value of 78db and 88db respectively providing 12.5 effective no.of bits(ENOB). The SAR ADC consumes a total power consumption of 2.4uW where latched comparator consumes 75% of power, DAC consumes 20% and SAR control logic consumes 5% of power. The important benchmarks of SAR ADC are defined as Figure-of-Merit (FOM) $=P_{total}/(2^{ENOB} * fs)$, where ENOB, P_{total} and fs are Effective Number of Bits, Total Power consumption and Nyquist frequency.

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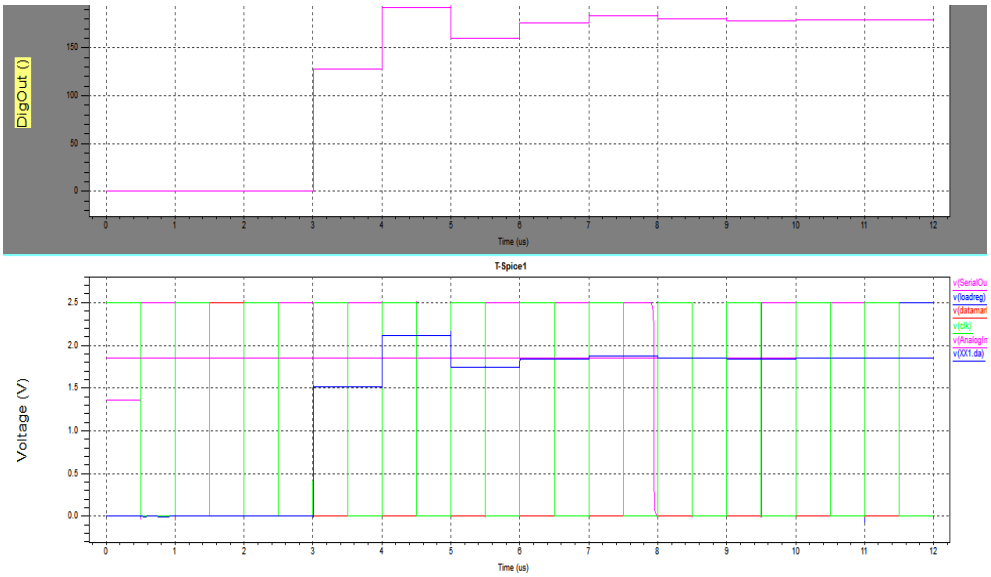


Fig. 6: Transient Analysis of Proposed SAR ADC.

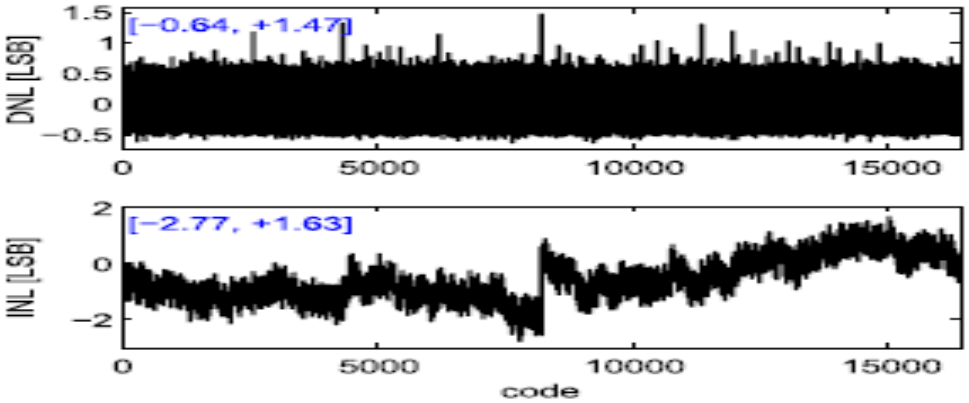


Fig. 7: Measurement of Static Performance of SAR ADC.

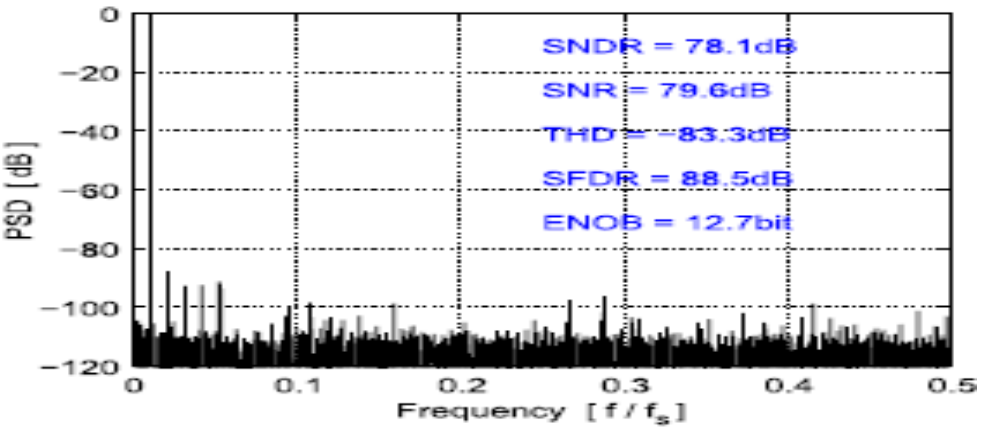


Fig. 8: Measurement of Dynamic Performance of SAR ADC.

Also the table I shows the comparison performance of proposed SAR ADC with other architectures.

Table 1: Performance Comparison

	[2]	[4]	[6]	[9]	[10]	In this work
Technology (um)	0.09	0.09	0.065	0.045	0.180	0.065
Resolution (bits)	13	14	14	14	18	14
Sampling rate(S/s)	51M	127K	82M	37M	6M	10K
Supply voltage(v)	1.2	1.5	1.2	2.2	5	1
DNL	-	-	-	-	-	-0.6/+1.4LSB
INL	-	-	-	-	-	-2.7/+1.6LSB
SFDR(db)	84	87.1	80.3	90	-	88
SNDR(db)	69.1	79.1	71.3	74.4	-	78
Power(w)	3.9m	1.67u	32.2m	56.6m	32.82m	2.4u
ENOB(bits)	11.6	13	11.8	12.1	-	12.6
FOM(fJ/conv. Step)	36	23	129	363	88	40

4. Conclusion

In this work, a 14b 10kS/s SAR ADC has been implemented for cardiac IMDs in 65nm CMOS technology.To minimize power consumption, a new power and noise efficient latched comparator has been proposed.The proposed ADC achieves a power consumption of 2.4uW.It utilizes a non-binary weighted capacitive array whose value is rounded to nearer integer value. The uniform geometry of DAC helps to enhance the linearity of ADC. The INL is between -2.7/+1.6 LSB and DNL is between -0.6/+1.4LSB. The FOM of ADC is 40fJ/conv. Step which is comparable with existing ADC topologies.

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