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Research Paper

Low power synthesis for asynchronous FIFO using unified power format (UPF)

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Abstract

Low power Design is the challenge for the current SoC Designers. With the growing complexity of the chips and the shrinking technology, power consumption in ASIC's has become a major challenge for the ASIC Engineer. The low power challenge is at every level of the ASIC Design flow. The low power techniques are applies at the Micro architecture level, RTL Design Level, Functional Verification level, Logic Synthesis level, Design for Test level, and Physical Design level. Nowadays, with the complexity gradually increasing at the SoC level, some of the EDA companies like Synopsys and Cadence are integrating the low power techniques in the tool itself. For instance, the two most commonly used low power flows are Unified Power Format (UPF) and Common Power Format (CPF). The Unified power format is from Synopsys flow while the Common Power format is from Cadence flow. In this paper, the emphasis is on reducing power by taking an Asynchronous FIFO with two separate clocks and applying the Unified power format flow in it. This paper presents the results of the research reported by the Synopsys Design Compiler before applying the UPF flow and after applying the UPF flow.

Keywords: *Clock Gating; Common Power Format (CPF); FIFO; Logic Synthesis; Low power; RTL Coding; Synchronous and Asynchronous Designs; Unified Power Format (UPF).*

1. Introduction

Logic Synthesis is the process of converting the RTL Code into gates or Net list. The inputs to any Synthesis flow would be as follows:

a) RTL Code (VHDL or Verilog)
b) Technology Libraries
c) Synopsys Design Constraints (SDC)

RTL Code is written typically in VHDL or Verilog and after mapping to the technology libraries with applying proper SDC, Net list is generated which will be in the form of logic gates. The power consumed in the circuit can be got from the net list. Without applying any UPF or CPF flow, the average power consumed by the design can be reported by the Synopsys Design Compiler (DC) tool. However, by applying any of the low power methodology flows, the low power report can be generated using the report power option in the Synopsys DC tool.

UPF flow that can be applied during Low Power Synthesis is as follows:

a) Creating Power Domains
b) Clock Gating
c) Special cell insertion
d) Retention Cells
e) Compile

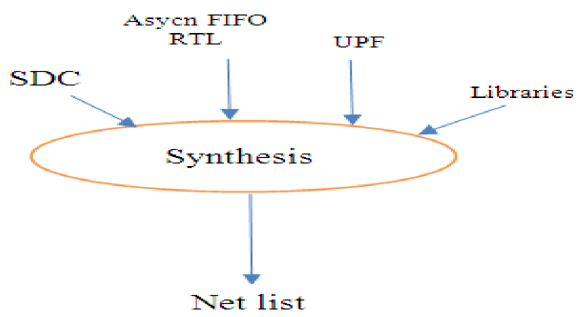

Fig. 1: A Typical Synthesis Flow with UPF.

1.1. Need of UPF

- UPF provides the ability to consider power as a key consideration in the initial process itself.
- No HDL supports the specification of power distribution and power management like UPF.
- Vendor specific formats are non-portable and chances of bugs will be more due to inconsistent specifications.

2. Design and implementation of asynchronous low power FIFO

FIFO is First-in First-out memory storage element. Its basic property is not only to store data but also to synchronize the data between two different clock domains. They are extremely useful in high speed data transfers. The main difference between Synchro-

nous and Asynchronous FIFO's is that Synchronous FIFO runs on a single clock while Asynchronous FIFO operates on two clocks. In other words, in Synchronous FIFO both the transmitter and receiver access the data on the same clock. This means that a master or the transmitter should provide the clock signal to all the receivers in the synchronous data transfers. In the asynchronous data transfer, there is no common clock between the transmitter and the receiver. The transmitter operates on its own clock while the receiver operates on its own clock. Hence, synchronization between the transmitter and the receiver becomes the challenge here. The synchronization information may be added to every byte of data or to every frame of data. Asynchronous data transfers are generally faster than synchronous data transfers as they operate on two different clocks.
This Asynchronous FIFO design has been implemented using a Novel Architecture which has already been published in previous papers. The RTL Code is taken as input in this paper and implemented using UPF flow. One can easily say that it can be termed as Power Aware Synthesis Flow. The Library requirements for the implementation of this Low Power Asynchronous FIFO are:

- Level Shifters
- Isolation Cells
- Retention Registers
- Power Switch Cells
- Power / ground pin definitions are required for all cells in a library
- Defined as attributes in .lib
- Allows accurate definition of multiple power / ground pin information

Fig. 2: Clock Domains in Asynchronous FIFO.

The inputs to the Synopsys Design Compiler are:
1)Asynchronous FIFO RTL Code in Verilog
2)Technology Libraries
3)Synopsys Design Constraints (SDC)
4)Unified Power Format (UPF) File
All the above files are inputs to the Design Compiler tool and the output of the flow is the Asynchronous FIFO Net list in Verilog format. This net list has all the UPF flow embedded as well as the constraints applied.

3. Experiment results

This experiment is carried out in two steps. One is before applying UPF and the other is after applying UPF.
Before applying UPF, the results of power report are as follows:
Global Operating Voltage = 0.95
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000ff
Time Units = 1ns
Dynamic Power Units = 1uW (derived from V, C, T units)
Leakage Power Units = 1pW
Cell Internal Power = 215.2753 uW (98%)
Net Switching Power = 5.0164 uW (2%)
Total Dynamic Power = 220.2917 uW (100%)

Table 1: Power Report before Applying UPF

Power Group	Internal Power(uW)	Switching Power (uW)	Leakage Power (pW)	Total(% Attrs) (uW)
IO_pad	0.0000	0.0000	0.0000	0.0000 (0.00%)
Memory	0.0000	0.0000	0.0000	0.0000 (0.00%)
Black_box	0.0000	0.0000	0.0000	0.0000 (0.00%)
Clock_network	0.0000	0.0000	0.0000	0.0000 (0.00%)
Register	207.2149	0.8666	2.8368e+07	236.4497 (86.13%)
Sequential	0.6216	0.6870	1.1146e+06	2.4233 (0.88%)
Combinational	7.4388	3.4627	2.4744e+07	35.6453 (12.98%)
Total	215.2753	5.0164	5.4227e+07	274.5183

After applying UPF, the results of the power report is as follows:
Global Operating Voltage = 0.95
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000ff
Time Units = 1ns
Dynamic Power Units = 1uW (derived from V, C, T units)
Leakage Power Units = 1pW

Table 2: Power Report after Applying UPF

Power Group	Internal Power (uW)	Switching Power(uW)	Leakage Power (pW)	Total(% Attrs) (uW)
io_pad	0.0000	0.0000	0.0000	0.0000 (0.00%)
Memory	0.0000	0.0000	0.0000	0.0000 (0.00%)
Black_box	0.0000	0.0000	0.0000	0.0000 (0.00%)
Clock_network	1.5809	10.9367	3.9345e+04	12.5569 (6.56%)
Register	104.6507	0.4741	3.9497e+07	144.6217 (75.60%)
Sequential	0.4318	0.4630	1.1462e+06	2.0410 (1.07%)
combinational	5.4918	2.3266	2.4261e+07	32.0796 (16.77%)
Total	112.1553 uW	14.2003 uW	6.4944e+07 pW	191.2992 uW

Cell Internal Power = 112.1552 uW (89%)
Net Switching Power = 14.2003 uW (11%)
Total Dynamic Power = 126.3556 uW (100%)
Cell Leakage Power = 64.9436 uW
From the comparison of power reports from table 1 and table 2, it is evident that power consumption of Asynchronous FIFO has been reduced by nearly 30%.

4. Conclusion

As, we can see from the above results, when the UPF flow is applied as the input to the Verilog file, the power has reduced from 274.51 uW to 191.29 uW almost 1.43 units decrease in power consumption. If this is the case of power reduction in a single component like an Asynchronous FIFO in an entire SoC, then it is up to the imagination of the SoC designer who can apply the Unified power format flow to reduce the power in the entire SoC which has many instances of FIFO's, peripherals, microcontrollers, microprocessor and Analog circuitry. Hence, this experiment clearly shows that UPF flow is very useful in reducing power at the IP level or at the SoC level.

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