International Journal of Engineering & Technology, 7 (1.1) (2018) 482-485

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Implementation of MHLFF based low power pulse triggered flip flop

Shreya Verma[1*], Tunikipati Usharani[2], S Iswariya[3], Bhavana Godavarthi[4]

[1,4] *Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Hyderabad, India-500043*

[2,3] *Department of Electronics and Communication Engineering, St. Peter's Engineering College, Hyderabad, India*

*Corresponding author E-mail: shreya.sverma.verma9@gmail.com

Abstract

The present research paper proposes to implement a low power pulse-triggered flip-flop. The proposed design is MHLFF (modified hybrid latch flip-flop). In MHLFF method, the pulse generator will be altered concerning illustration inverters what's more a pasquinade transistor. This technique will be comparative should understood kind about flip flop what's more it utilizes a static lock structure. Should succeed Most exceedingly bad situation delay issue brought on Eventually Tom's perusing discharging way comprise from claiming three stacked transistor MHLFF may be presented. We can minimize the power and delay when compared to the existing models i.e, CDFF and SCDFF. The circuit was implementing using Cadence Virtuoso tool in 90-nm and 45-nm technology

Keywords: *Flip flop, Low power, Pulse triggered, Cadence.*

1. Introduction

The low power pulse-triggered flip-flop. The proposed design is MHLFF (modified hybrid latch flip flop).In MHLFF method, that pulse generator may be changed Likewise inverters What's more an pasquinade transistor. This system is comparative should understood sort of flip flop Furthermore it utilizes a static lock structure. On beat Most exceedingly bad case delay issue brought on Eventually Tom's perusing discharging way comprise from claiming three stacked transistor MHLFF will be acquainted [1]. We can minimize the power and delay when compared to the existing models i.e, CDFF and SCDFF. The circuit was implementing using Cadence Virtuoso tool in 90-nm and 45-nm technology. Those recommended outline adopts An indicator feed-through technobabble should enhance this delay. Comparable of the Static-Configured-FF plan (SCDFF) design, the suggested outline likewise utilizes a static lock structure Furthermore a restrictive release plan on dodge superfluous exchanging during a inner hub [2]. However, there need aid three significant contrasts that prompt a interesting TSPC lock structure Also aggravate the suggested configuration different from those past particular case.

In An feeble pull-up PMOS transistor MP1 with entryway associated with the ground may be utilized within the main phase of the TSPC lock. This provides for Ascent will An pseudo-NMOS rationale style design, and the charge guardian out for those inward hub X could make spared. Furthermore of the out simplicity, this approach additionally diminishes the load capacitance of hub X. Second, an pasquinade transistor MNx controlled Toward the pulse clock is incorporated so that data information could drive hub Q of the lock specifically (the indicator feed-through scheme) [11]. Alongside the pull-up transistor MP2 at those second stage inverter of the True-Single-Phase-Clock (TSPC) latch, this addi tional acceptably facilitates assistant sign crashing starting with those information sourball with hub Q. The hub level camwood subsequently be rapidly pulled dependent upon abbreviate the information move delay.

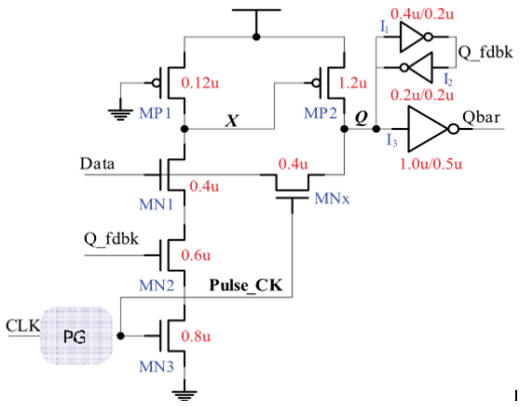

Figure.1: Schematic of the pulse triggered FF design

Third, the pull-down organize of the second phase inverter may be completely uprooted. Instead, that recently utilized pasquinade transistor MNx gives a discharging way. Those part assumed Eventually Tom's perusing MNx may be accordingly two-fold, i. E. , giving work to additional crashing with hub Q Throughout 0 on 1 information transitions, Furthermore discharging hub Q Throughout "1" with "0" information transitions. Compared with the lock structure utilized within SCDFF design, the out investment funds of the recommended outline incorporate a accuse guardian (two inverters), a pull-down organize (two NMOS tran-

Copyright © 2018 Authors. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

sistors), and a control inverter. The just additional part acquainted will be an NMOS pasquinade transistor will back sign encourage through. This plan really enhances the "0" with "1" delay What's more hence diminishes that dissimilarity the middle of those climb time and the fall time postponements [4].

2. Problem Identification

In the existing models the power consumption is more because of using implicit type of pulse triggering and also the number of transistors used is more. So, the speed of the circuit decreases and output is delayed. The proposed model uses explicit type of pulse-triggering so that the power consumption will decrease. And also we have provided the feedback .In this project we implement the flip-flop design in **90nm and 45nm** technology using CADENCE tool. As the technology is minimum the power consumption is minimum, area required for the circuit decrease and the speed of operation increases [5].

2.1 Existing Model

Conditional discharge flips flop (CDFF):
In this paper, high-octane flip-flops need aid investigated what's more classified under two categories: those restrictive precharge and the conditionals catch advances. This order will be In view of how with forestall alternately diminish the excess inward exchanging exercises [6]. Another flip-flop may be introduced: the restrictive release flip-flop (CDFF)..

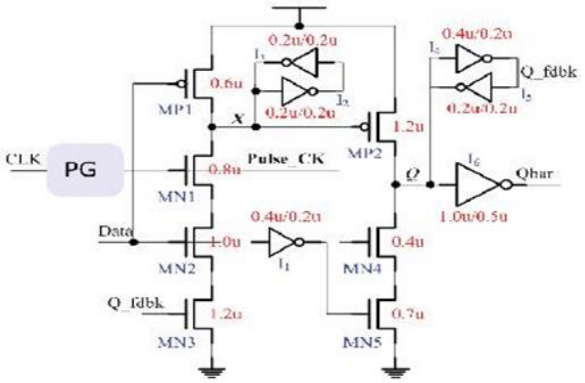

Figure. 2: Schematic of SCDFF

S-CDFF employments static lock structure and hence contrast starting with the CDFF. It doesn't comprise for periodical pre charges for inner hub. Fig 2. Indicates the schematic outline from claiming S-CD flip flop. It is Hosting a more data-to-Q delay similarly as contrasted with CDFF configuration. Those three transistors NMOS_1- NMOS_2 - NMOS_5 constitutes an discharging way which brings about Most exceedingly bad situation delay [7]. A bigger data-to-Q (D-to-Q) delay is exhibited Toward S-CDFF plan as contrasted with the CDFF outline.

3. Proposed Model

Those control utilization is critically essential over cutting edge VLSI circuits particularly for low-power provisions. Those force optimizations systems are connected at distinctive levels for advanced plan. However, streamlining during the rationale level will be a standout amongst the the vast majority important errands on minimize the energy. Around rationale components, latches Furthermore flip-flops would basic of the execution about advanced systems. In particular, D-type flip-flops (DFFs) need aid broadly utilized within memory plan Furthermore test requisitions. There would A percentage worries in the plan about DFF for example, Tclk-q (the delay starting with the edge about clock on yield about DFF), Cclk (load capacitance of the flip-flop clock), and the range. These parameters alongside the clock recurrence and the energy utilization of the flip-flop determine those generally performance of a DFF. Lessening Cclk alternately the recurrence of the clock need an incredible effect on the changing control utilization of the flip-flop clock tree [10].
Drawback of existing system using transmission gate (TG) power consumption is more and speed is less.

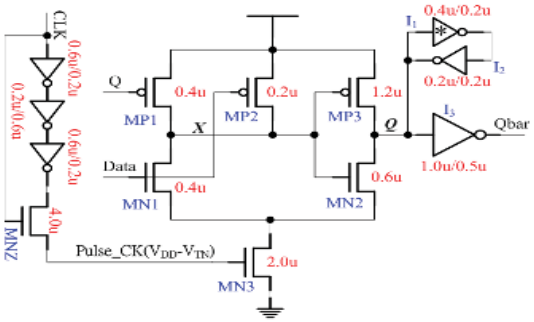

Figure.2.1: Schematic of MHLFF

The force utilization is critically vital clinched alongside advanced VLSI circuits particularly to low-power requisitions. The control optimizations systems are connected during distinctive levels for advanced outline. However, streamlining In the rationale level will be a standout amongst the the majority important assignments to minimize the force. Around rationale components, latches Furthermore flip-flops are discriminating of the execution from claiming advanced frameworks. For particular, D-type flip-flops (DFFs) need aid broadly utilized within memory outline furthermore test provisions. There are exactly worries in the plan from claiming DFF for example, Tclk-q (the delay starting with those edge for clock should yield from claiming DFF), clk (load capacitance of the flip-flop clock), and the region. These parameters alongside those clock recurrences and the control utilization of the flip-flop determine the general performance of a DFF. Lessening Cclk or that recurrence of the clock need an extraordinary effect on the dynamic energy utilization of the flip-flop clock tree [10] [12].
A great deal exert need been aggravated will enhance those execution of flip-flops, e. G. Those mixture lock flip-flop (HLFF), which will be An static, single-edge-triggered FF, need been suggested In light of generating an unequivocal transparency window the place the move will be permitted. It is comparable should a lock a direct result it camwood give a delicate clock edge which considers slack death the data, Furthermore henceforth minimizing those impact for clock skew on the cycle the long run. The fundamental hindrance for this circlet may be the presence from securing excess hub moves which actuate some energy dispersal. The semi-dynamic flip-flop (SDFF) recommended clinched alongside will be known as a quick flip-flop. It will be a single-edge-triggered FF What's more speedier over those HLFF [7].

Advantages of Proposed System

1. Speed of operation is more.
2. Power consumption is minimum.

4. Methodology

4.1 Pulse Generator

For providing clock signal to the input we place a pulse generator (PG) circuit and the output of the PG is then given as a clock to the circuit.
A pulse generator may be whichever a electronic out or a bit about electronic test supplies used to produce rectangular pulses. Pulse generators are utilized fundamentally to working for advanced circuits, related capacity generators are utilized principally for simple circuits [8].

Pulse generators fit about generating pulses with widths under more or less 100 picoseconds are often termed Likewise "micro-wave pulse" What's more commonly produce these ultra-short pulses utilizing venture recuperation diode (SRD) alternately non-linear transmission line (NLTL) strategies (for example). Step recuperation diode pulse generators are modest Be that as regularly oblige a few volts about enter drive level and bring An reasonably large amount about irregular jitter (usually undesirable variety in the time In which progressive pulses occur)..

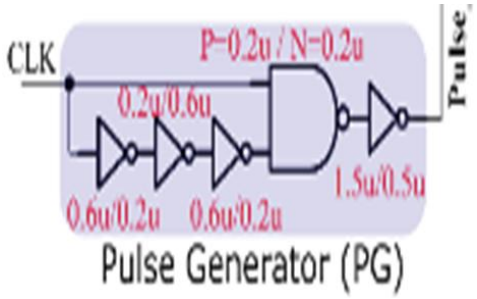

Figure.3: Pulse generator circuit

4.2 Pulse Triggering

Those yield of a flip flop might a chance to be transformed toward achieve a little change in the data indicator. This little change camwood be brought for the help of a clock pulse or usually known as a trigger pulse.

At such a trigger pulse will be connected of the input, those yield progressions Also consequently the flip flop will be said should a chance to be triggered. Flip flops would relevant for planning counters or registers which saves information in the type about multi-bit numbers. However such registers requirement an aggregation from claiming flip flops associated with one another as successive circuits. Furthermore these consecutive circuits oblige trigger pulses.
Those term pulse-triggered implies that information are entered under the flip-flop on the climbing edge of the clock pulse, yet the yield doesn't reflect those information state until those falling edge of the clock pulse [9].

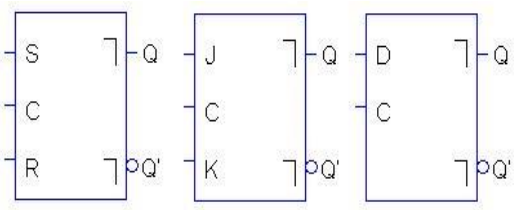

Figure.3.1: Basic pulse triggered flip-flops

Similarly as this sort of flip-flops are delicate should any change of the information levels Throughout the clock pulse is at present HIGH, those inputs must be set up former of the clock pulse's climbing edge What's more must not make changed in the recent past those tumbling edge. Otherwise, vague comes about will happen. The three fundamental sorts of pulse-triggered flip-flops are S-R, J-K What's more d. Their rationale images would demonstrated The following. Perceive that they don't have the changing information pointer toward those clock enter Be that as need postponed yield images at the outputs.

5. Results

5.1 Schematic design

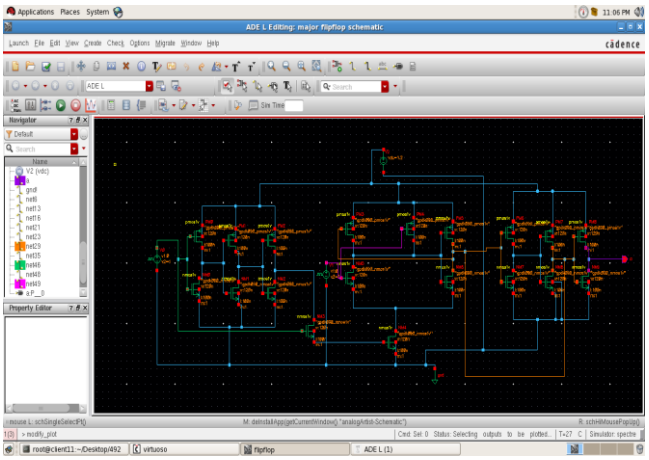

Figure.4: Final schematic design

a) Proposed Model Modified Hybrid Latch Flip-Flop (MHLFF) Outputs

Schematic of the proposed model in 90nm technology. Here the schematic of the flip-flop is shown. Transistors are connected according to the circuit and the connections are made accordingly .

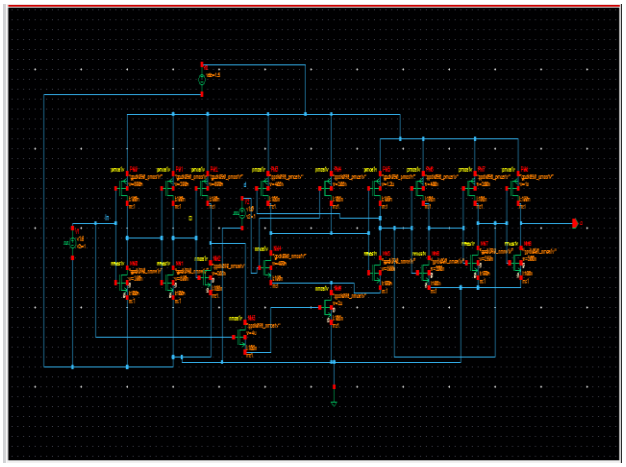

Figure.4.1: schematic of proposed model (MHLFF)

b) **Wave form of the above circuit**

The output waveforms are plotted and are shown below in the figure.

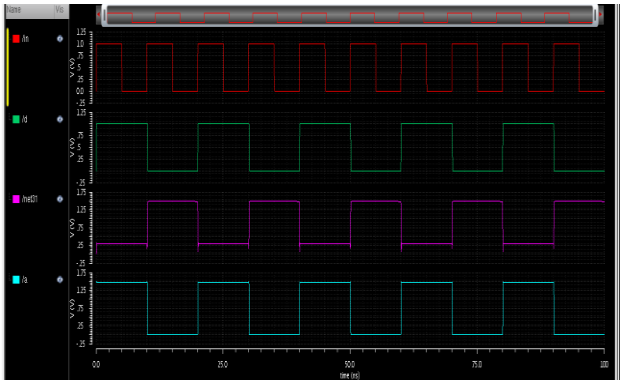

Figure.4.2: Waveforms of the proposed model MHLFF

c) Power calculation.

Power of the circuit = **187.9E-6**

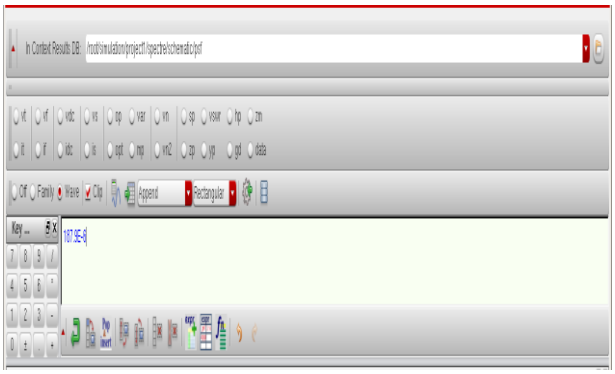

Figure.4.3: power calculation of MHLFF flip-flop

(d) Delay calculation

Delay = 169.6E-12

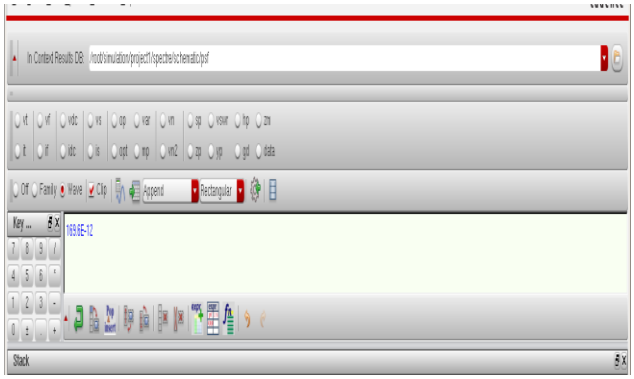

Figure.4.4 Delay Calculation flip flop

6. Conclusion

In this brief, we presented a modified hybrid latch flip flop (MHLFF) Outline Eventually perusing utilizing a lock structure incorporating a blended outline style comprising of pasquinade transistor Also pseudo-NMOS rationale. Those way permit might have been will furnish An sign bolster through starting with information wellspring of the interior hub of the latch, which might encourage additional crashing to abbreviate the move the long haul Also upgrade both force Furthermore pace execution. The configuration might have been intellectual elite attained toward utilizing An basic pasquinade transistor. Far reaching simulations were conducted, and the comes about destroyed backing those cases of the suggested configuration over Different execution parts.

Acknowledgement

The writer might want to much thanks to those division about department of science and technology and editorial manager and the unacknowledged reviewers to their valuable remarks what's more feedback.

References

[1]. Dekker, Cees; Tans, Sander J.; Verschueren, Alwin R. M. (1998). "Room-temperature transistor based on a single carbon nano tube". Nature. **393** (6680): 49–52. International Technology Roadmap for Semiconductors Archived August 25, 2011, at the Wayback Machine. 2009 Edition

[2]. H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998

[3]. K. Chen, "A 77% energy saving 22-transistor single phase clocking D-flip-flop with adoptive-coupling configuration in 40 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339

[4]. E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 482–483.

[5]. P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.

[6]. M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edge triggered flip-flop using an output-controlled discharge configura-tion," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 2429–2432.

[7]. S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single- and double-edge-triggered flip-flops for high speed applications," *IEE Proc. Circuits Devices Syst.*, vol. 152, no. 2, pp. 118–122, Apr. 2005.

[8]. S. Sadrossadat, H. Mostafa, and M. Anis, "Statistical design framework of sub-micron flip-flop circuits considering die-to-die and within-die variations," *IEEE Trans. Semicond. Manuf.*, vol. 24, no. 2, pp. 69–79, Feb. 2011.

[9]. M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus Clock Slope and impact on the clock network design," *IEEE Trans. Circuits Syst.*, vol. 57, no. 6, pp. 1273–1286, Jun. 2010

[10]. Ummadisetty Nagamani, Vydehi Merusomayajula, G Divya, Paparao Nalajala, Bhavana Godavarthi," Design of fault tolerant alu using triple modular redundancy and clock gating", Journal of Advanced Research in Dynamical and Control Systems Vol. 9. Sp– 17 / 2017

[11]. C Devi Supraja, E Vijaya Babu[2], Rohith Bala Jaswanth B, Paparao Nalajala, Bhavana Godavarthi,"Design and analysis of cnfet based 2:1 mux in nano scale region", Journal of Advanced Research in Dynamical and Control Systems Vol. 9. Sp– 18 / 2017